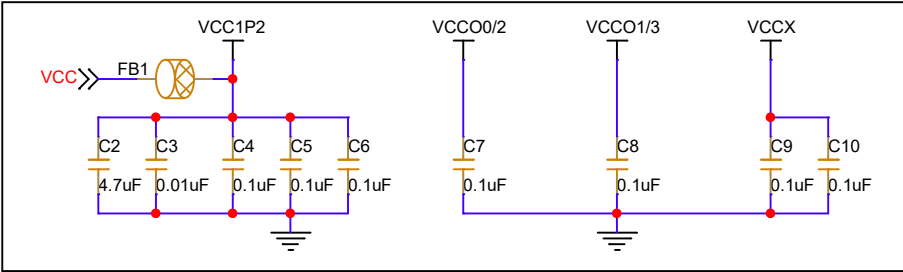
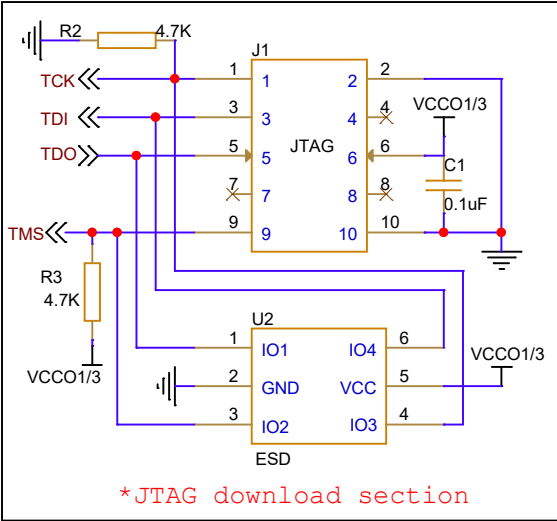
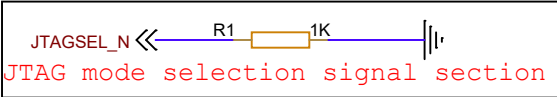
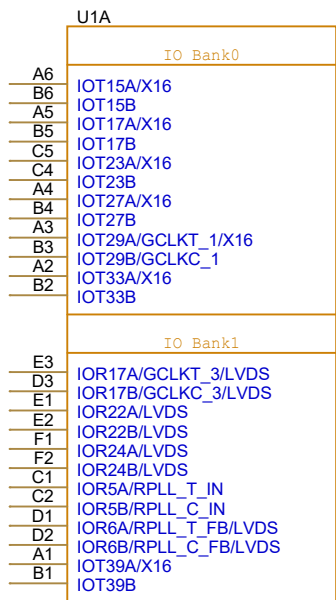
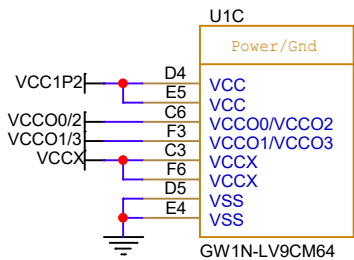
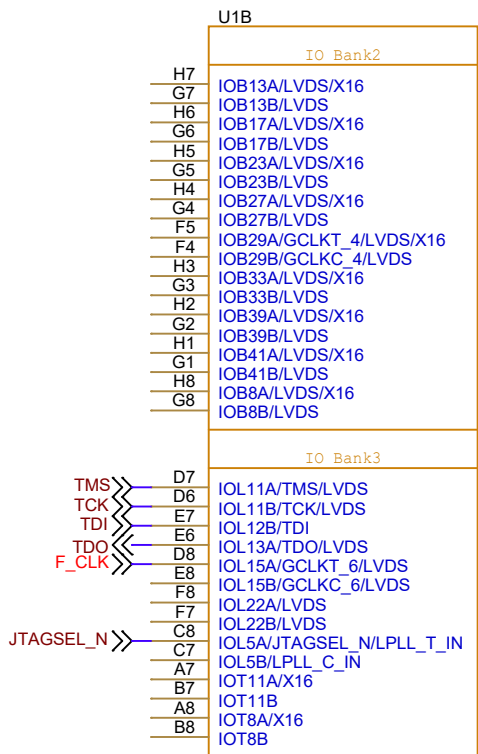
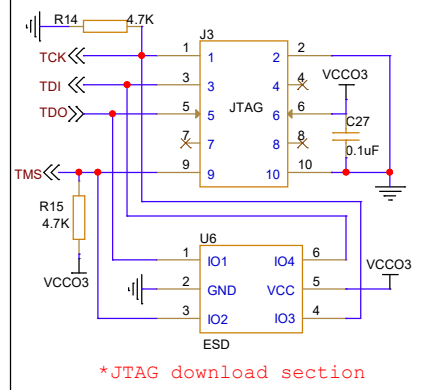
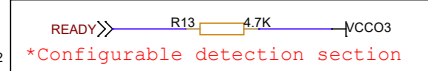
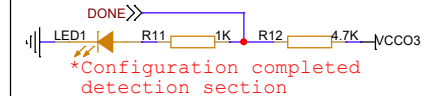
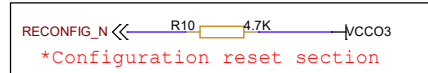
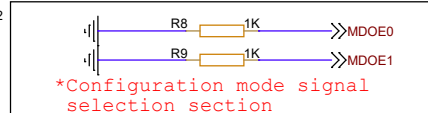
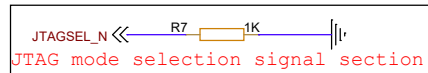
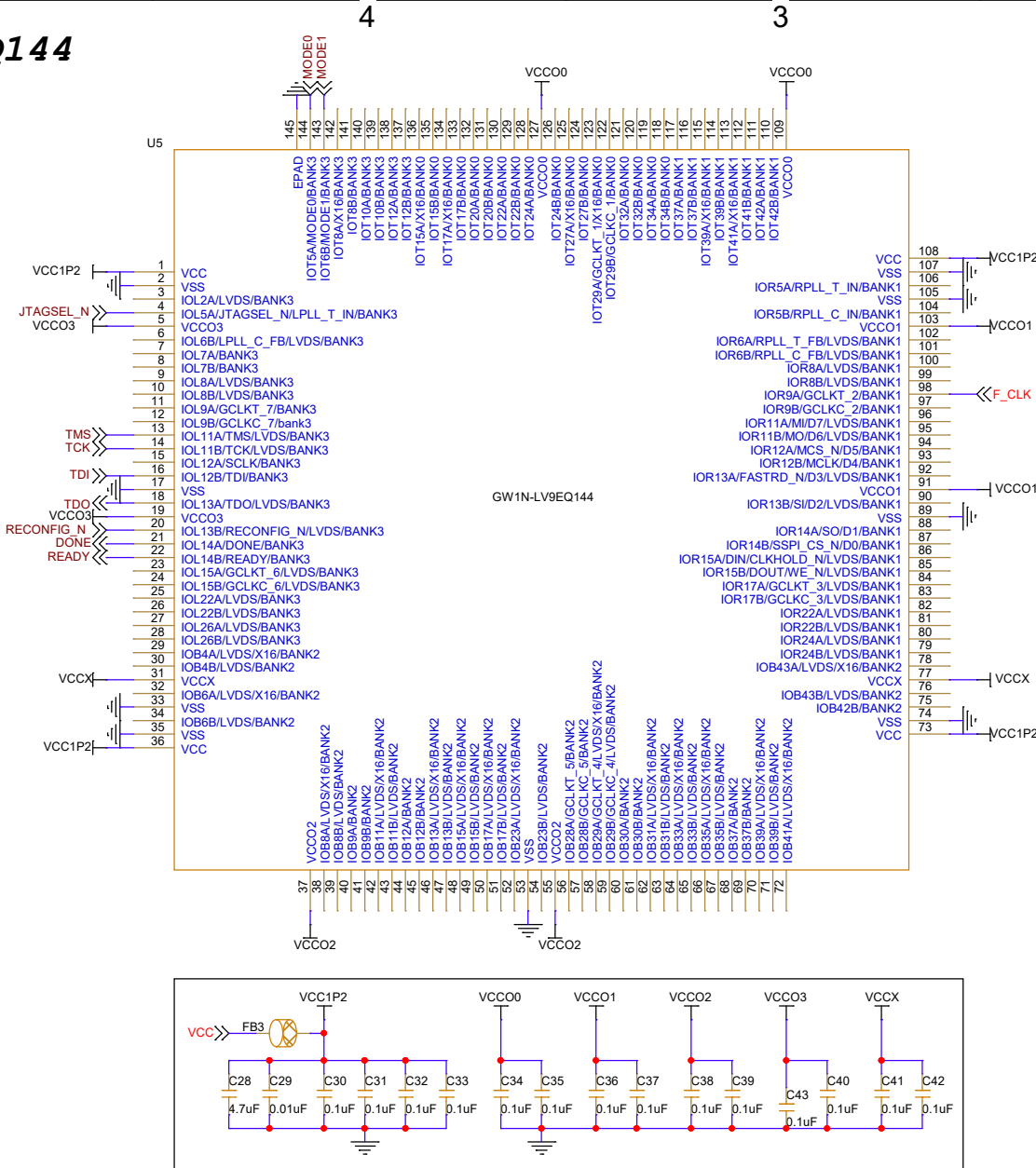


GW1N-LV9CM64

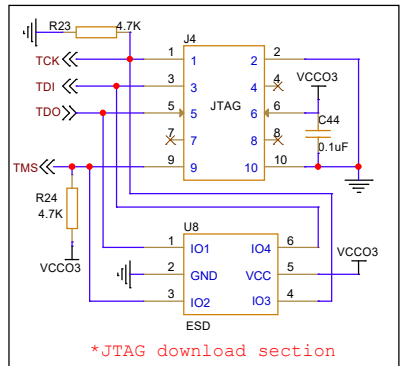
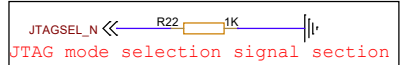
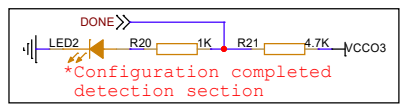
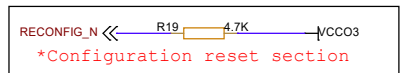
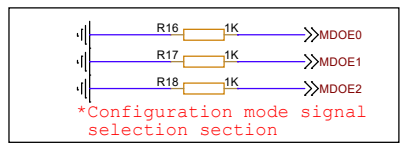
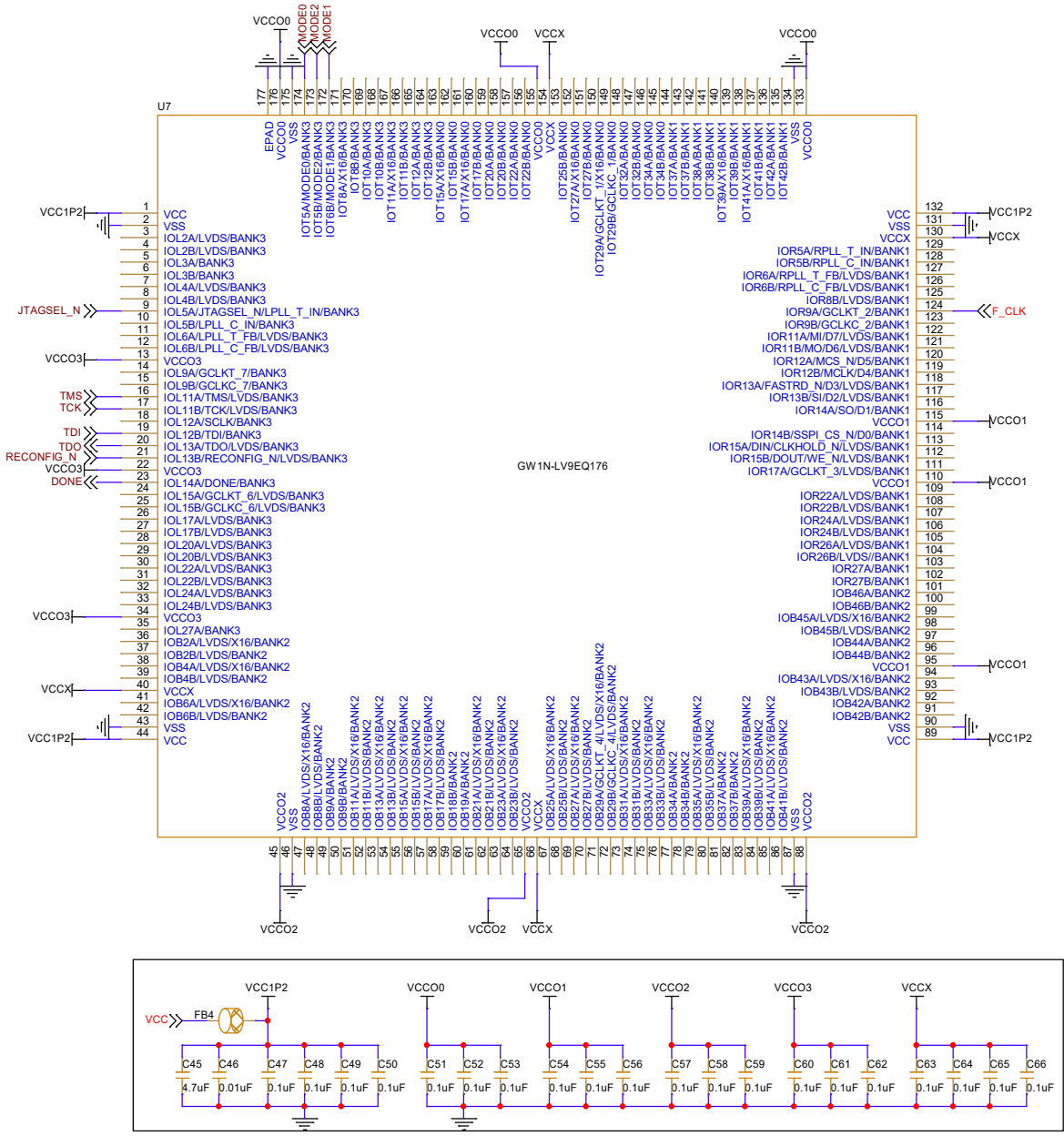


- Notes:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

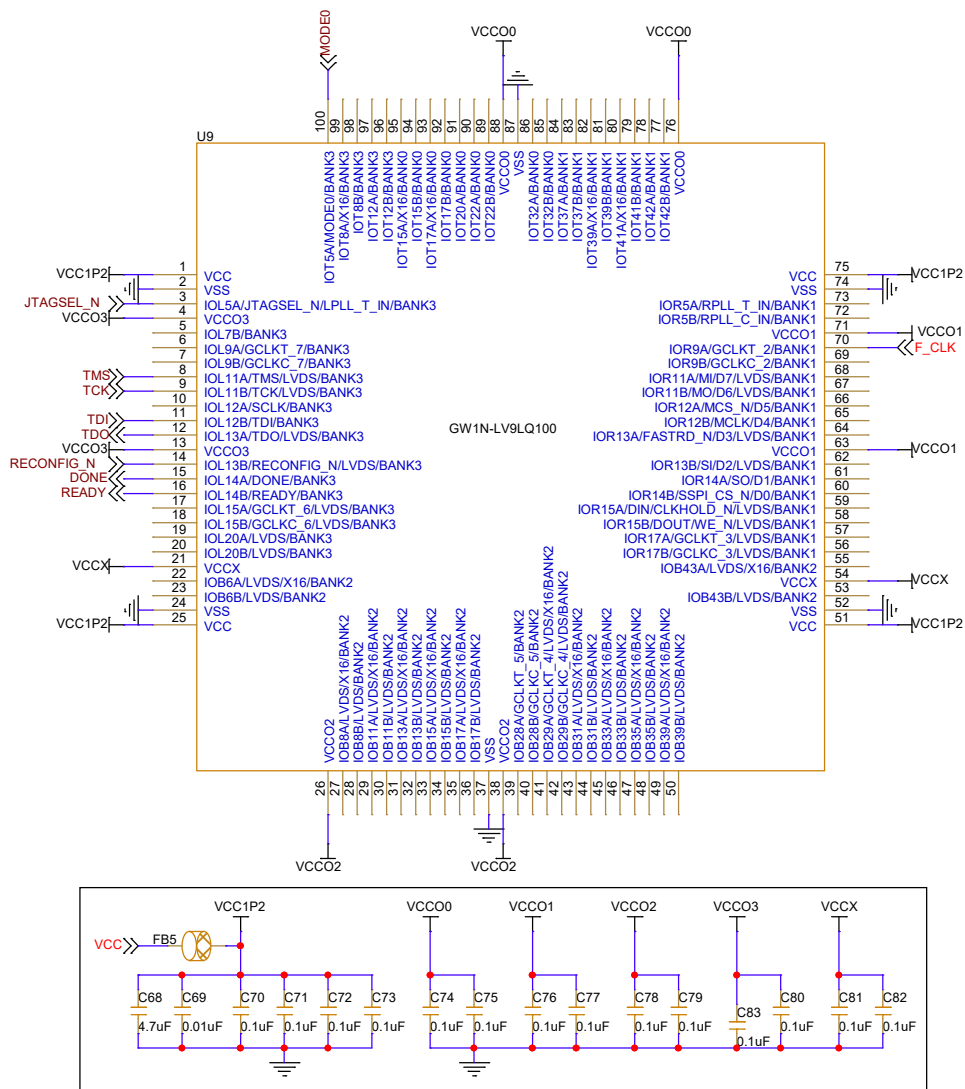


Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

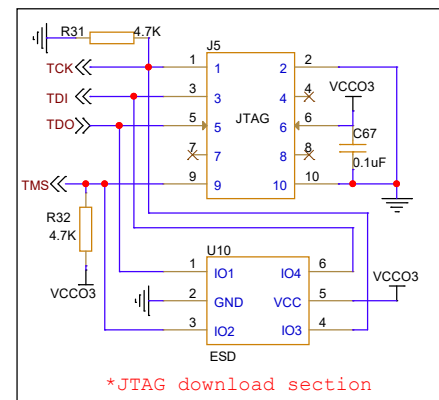
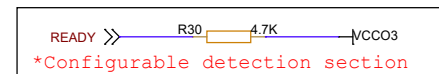
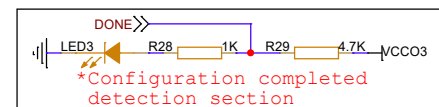
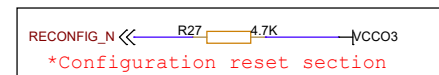
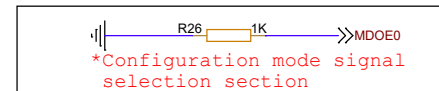
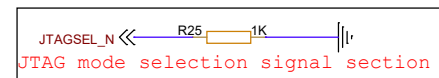
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GOWIN Minimum System Diagram		
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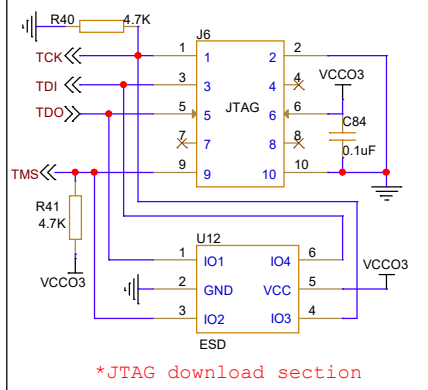
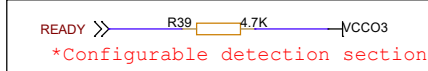
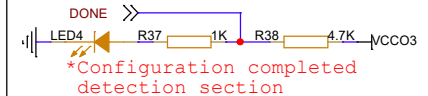
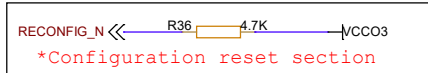
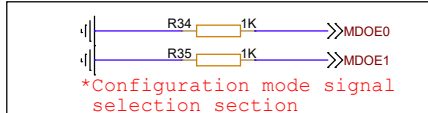
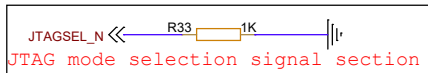
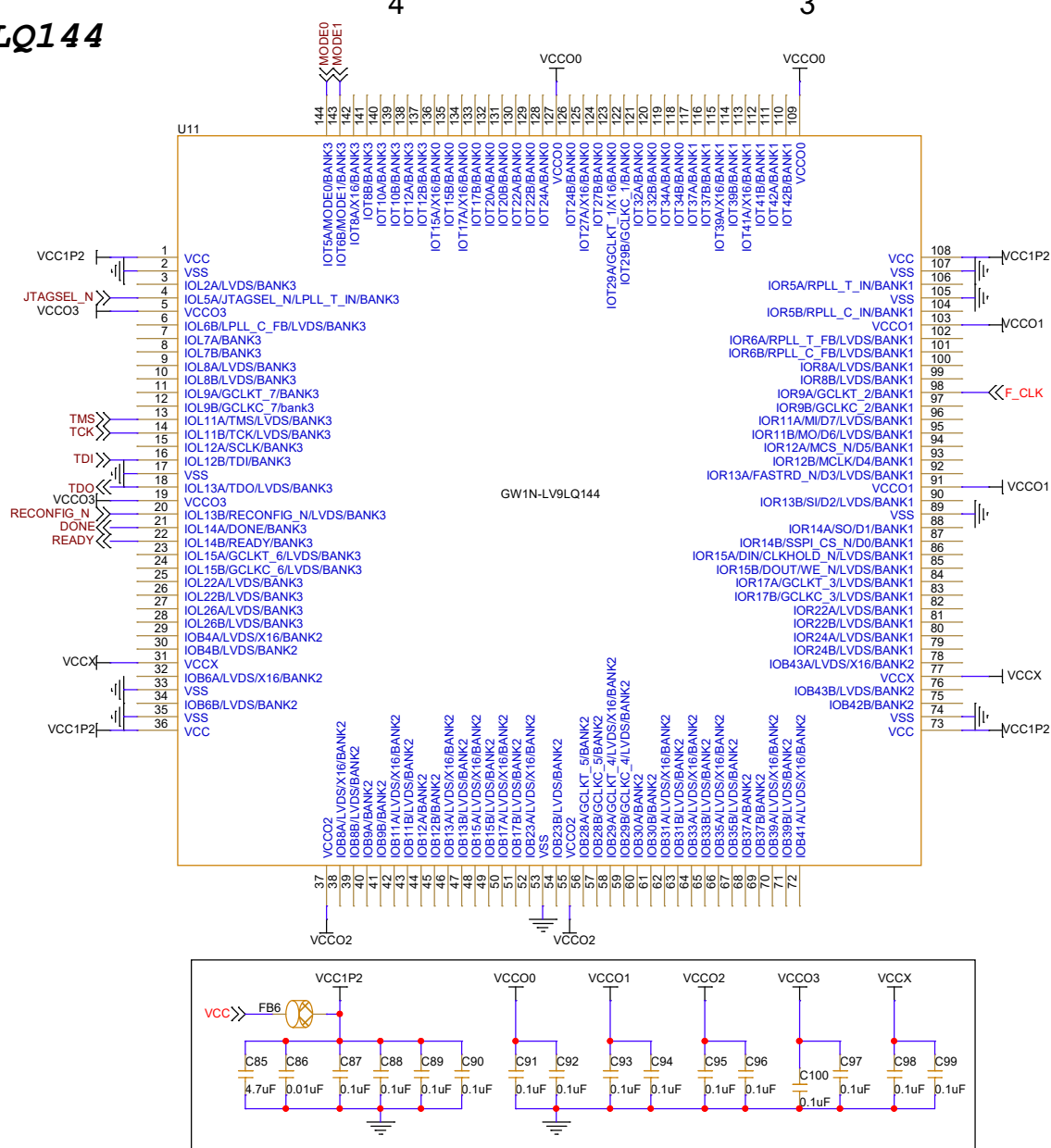
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection to the JTAG download circuit.



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



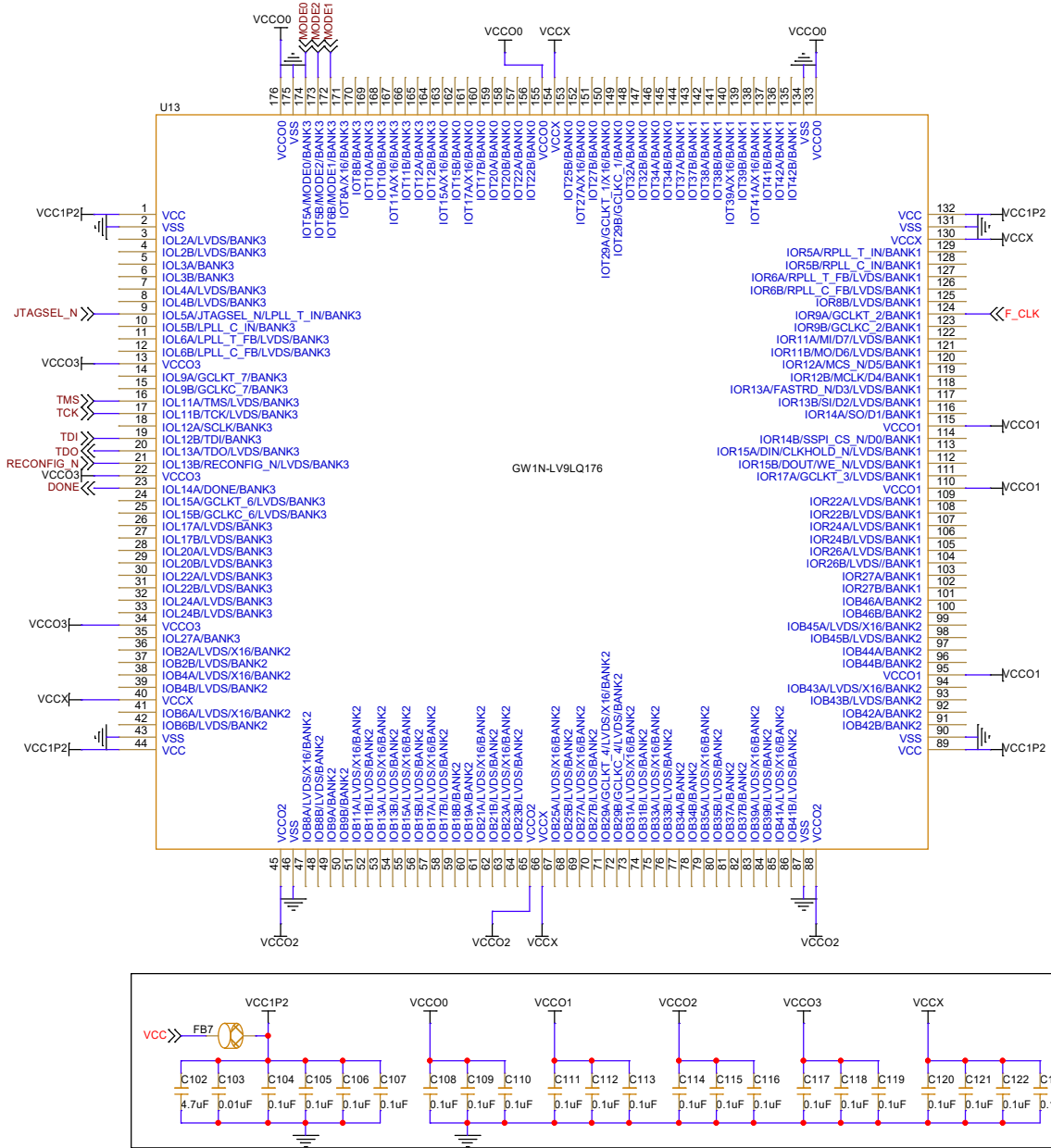
Title		
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Size	Document Number	Rev
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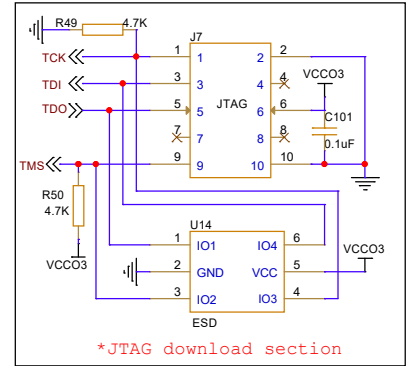
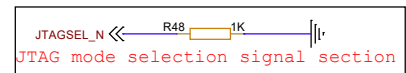
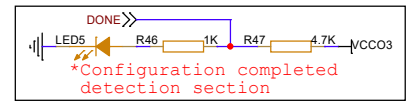
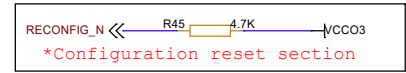
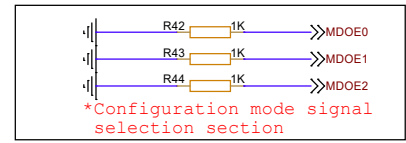
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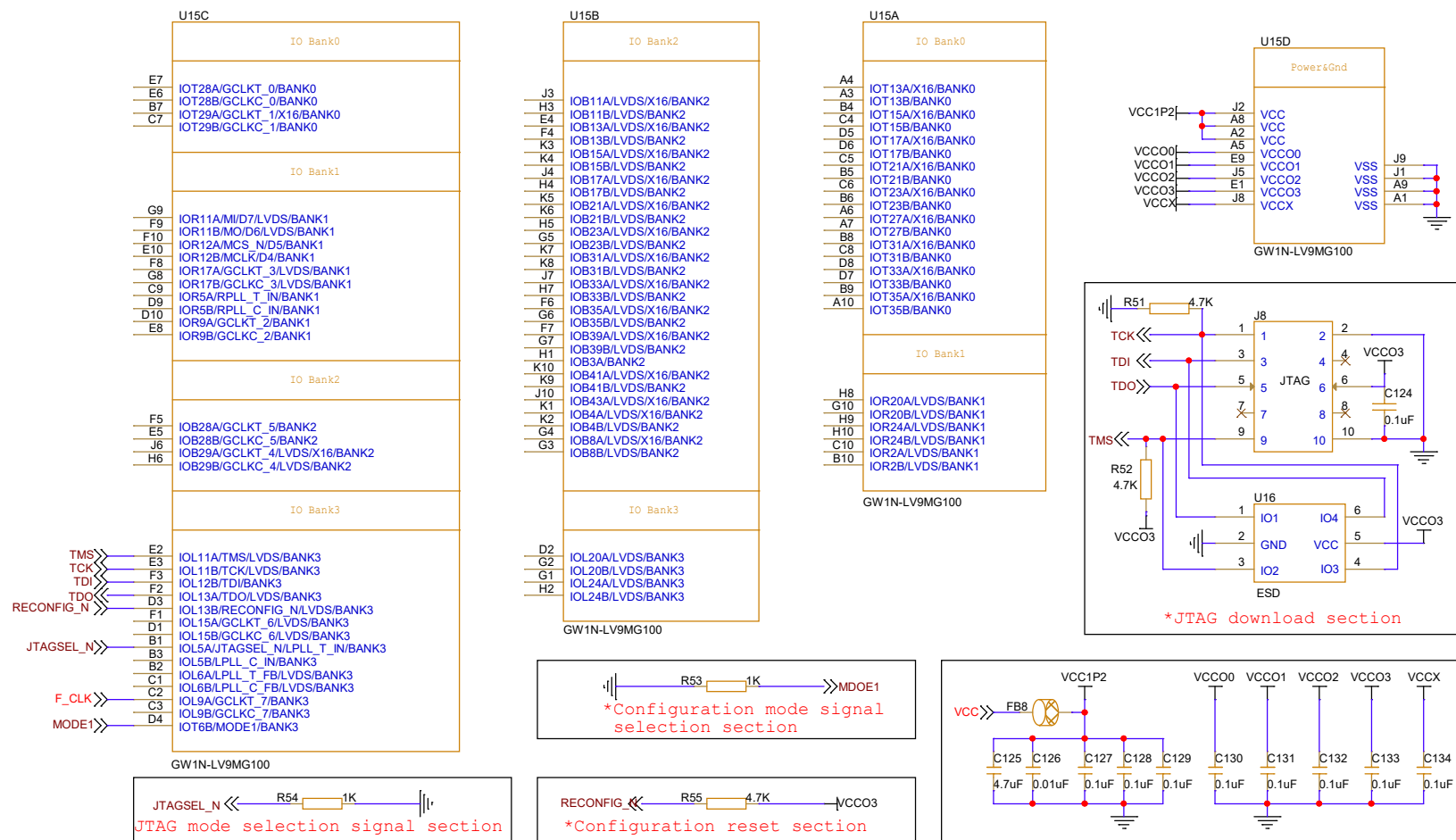
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.





Notes:

- NOTES:
- 1.F CLK signal is an external input clock signal.
 $\overline{IT}$ is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

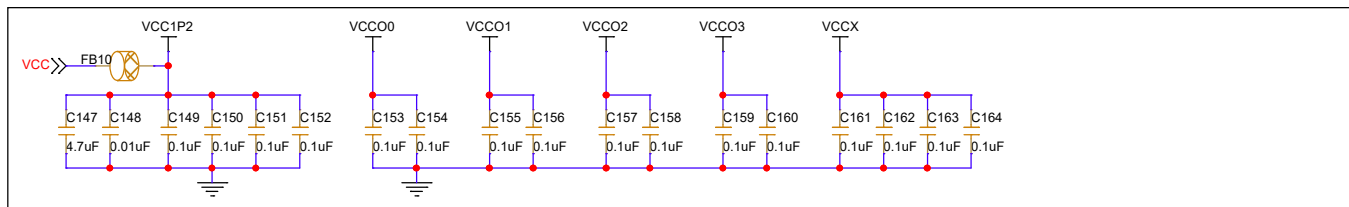
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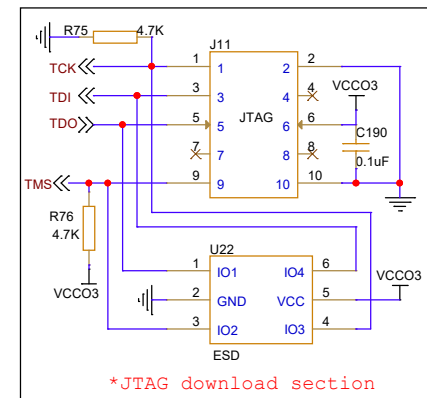
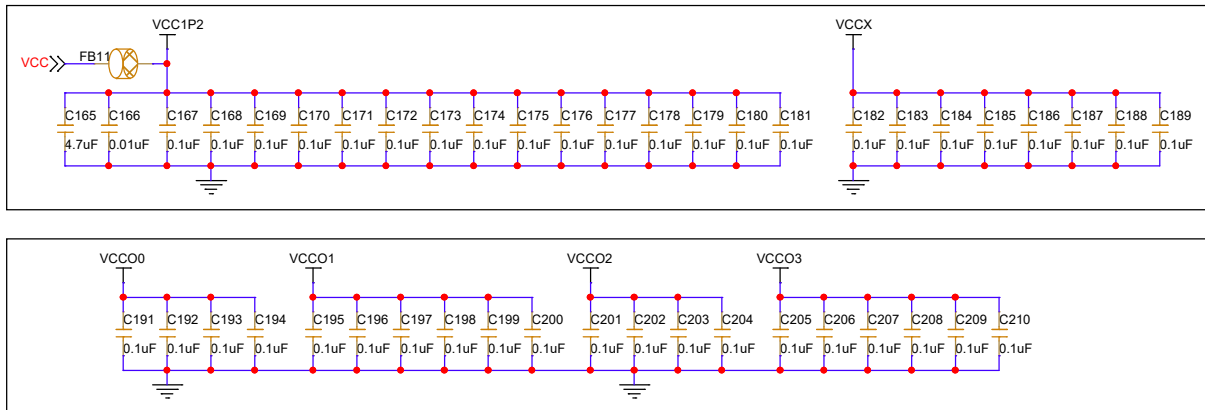
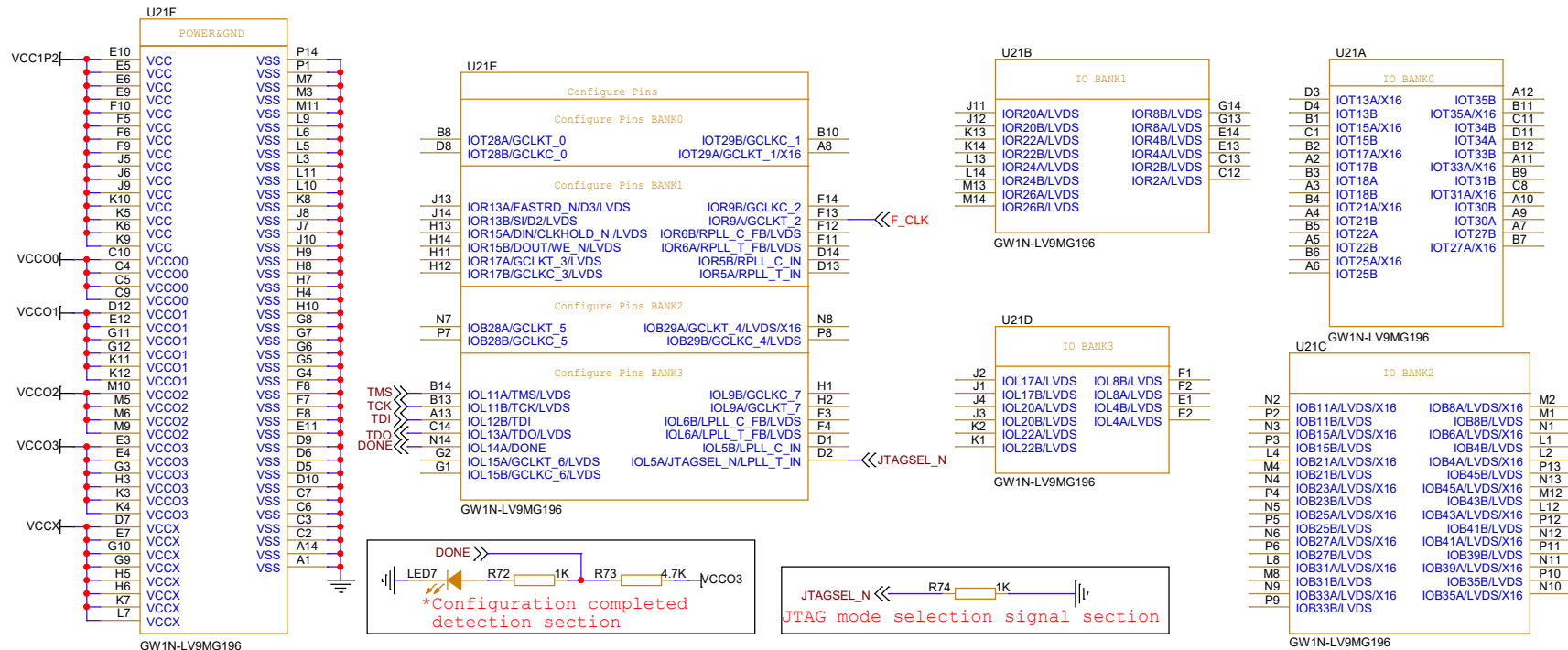
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A



Title			
GOWIN Minimum System Diagram			
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B	GW1N-LV9MG160		2.3
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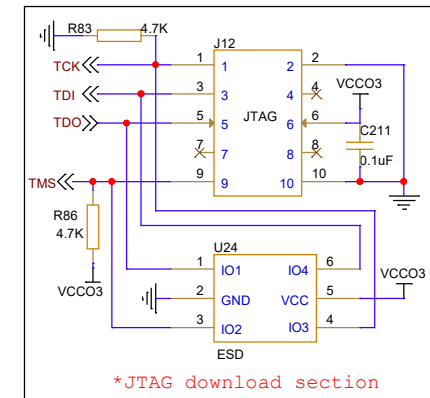
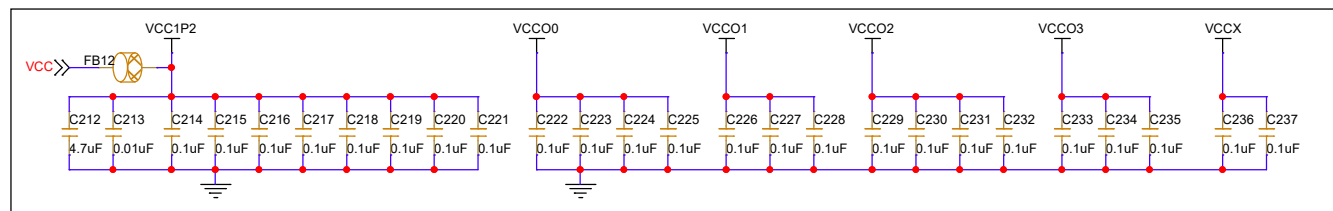
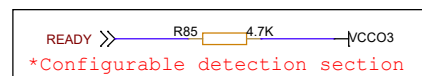
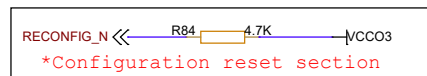
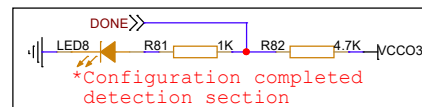
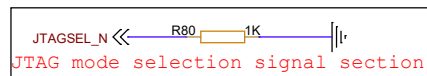
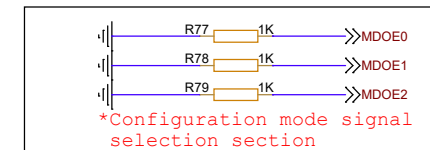
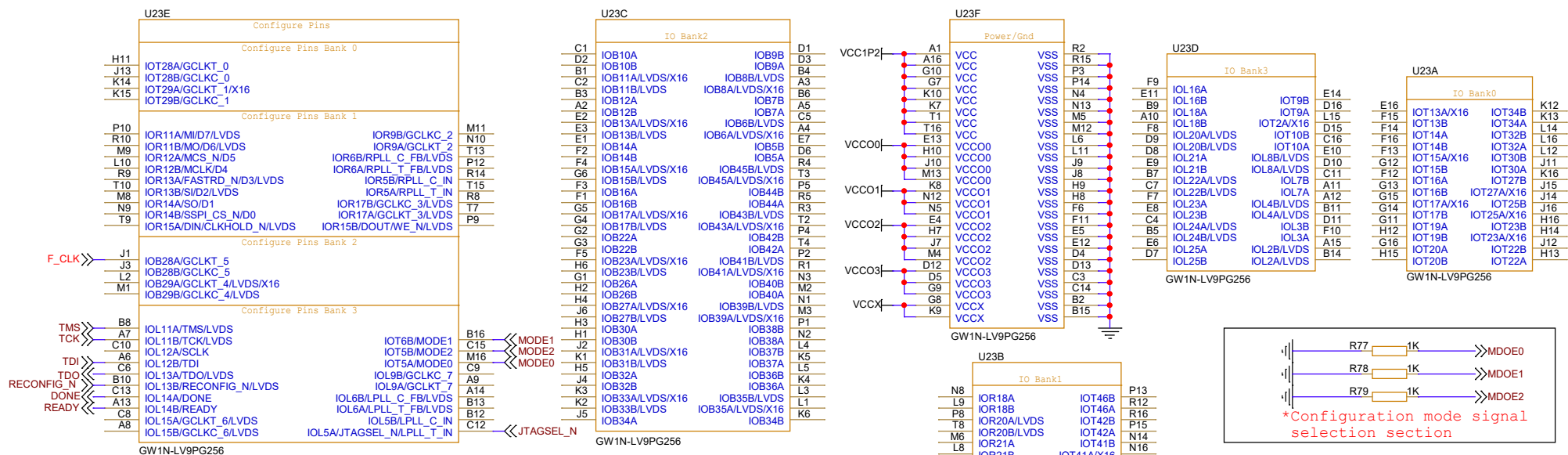


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9MG196	2.3
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5
GW1N-LV9PG256



Notes:

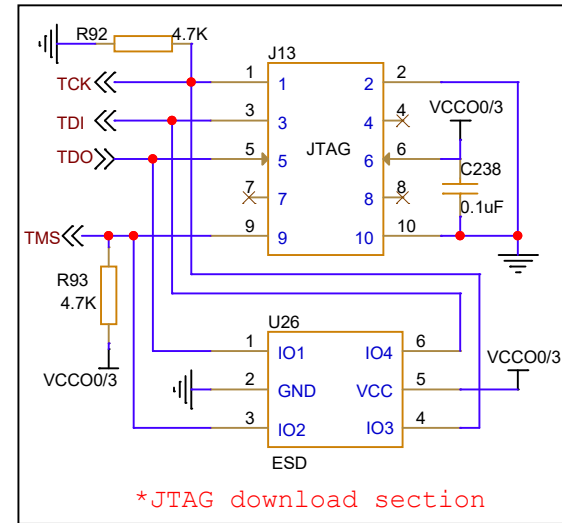
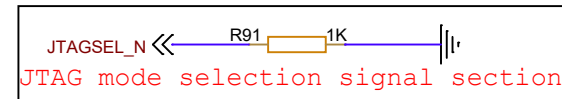
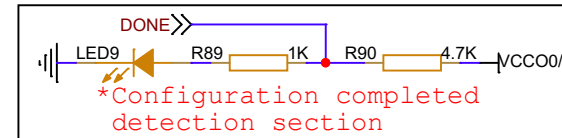
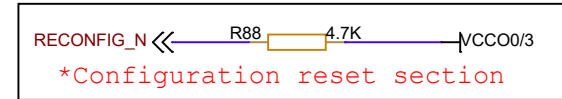
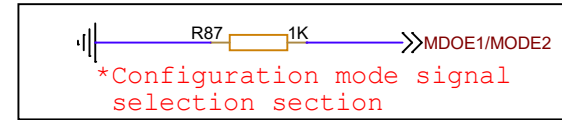
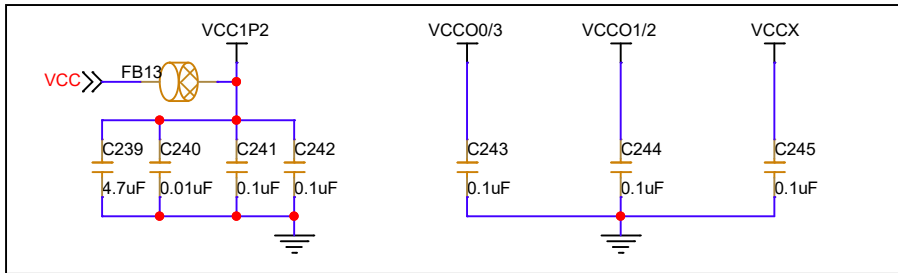
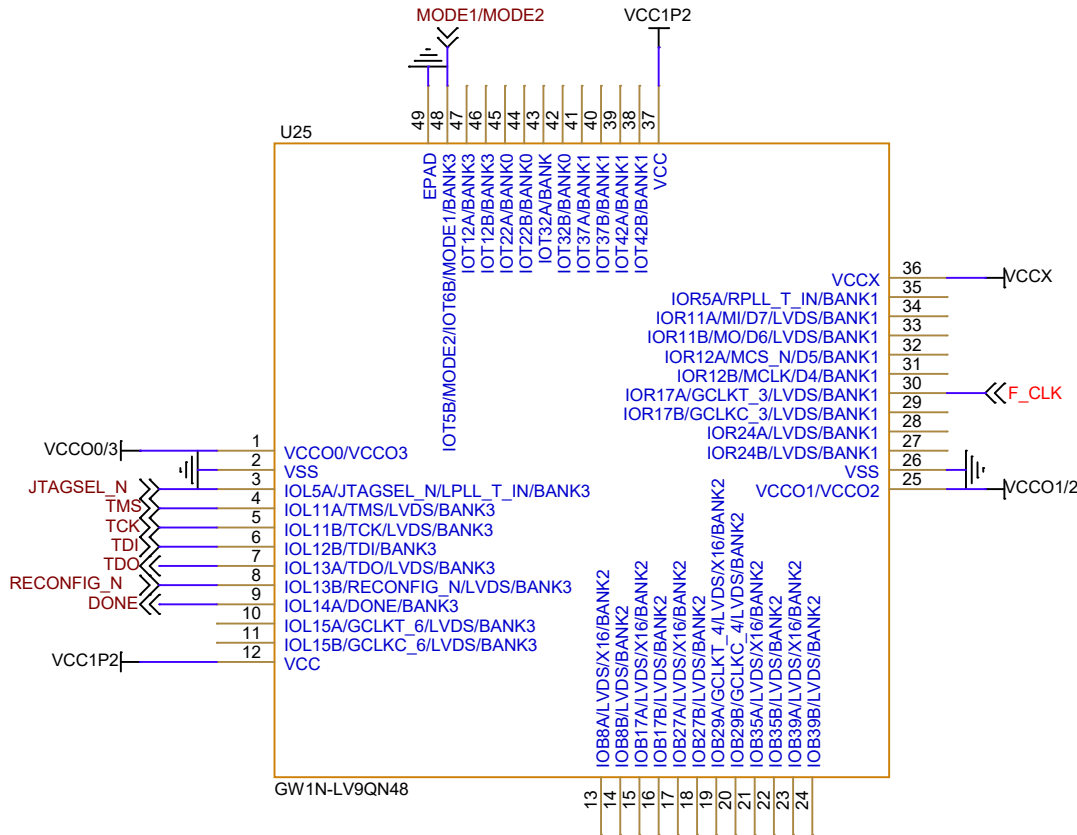
1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title				
GOWIN Minimum System Diagram				
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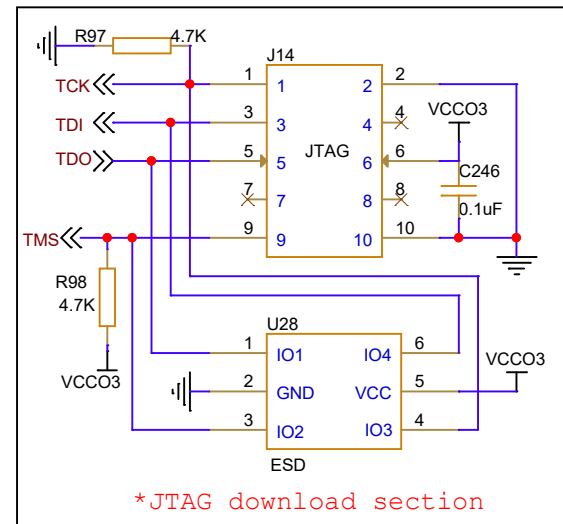
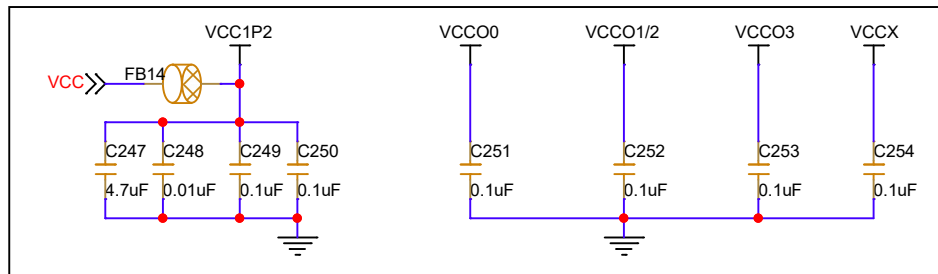
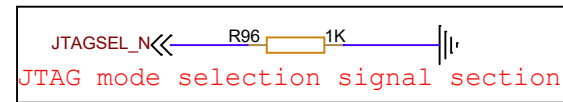
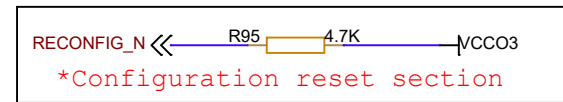
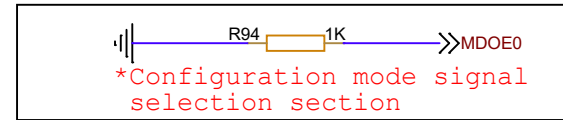
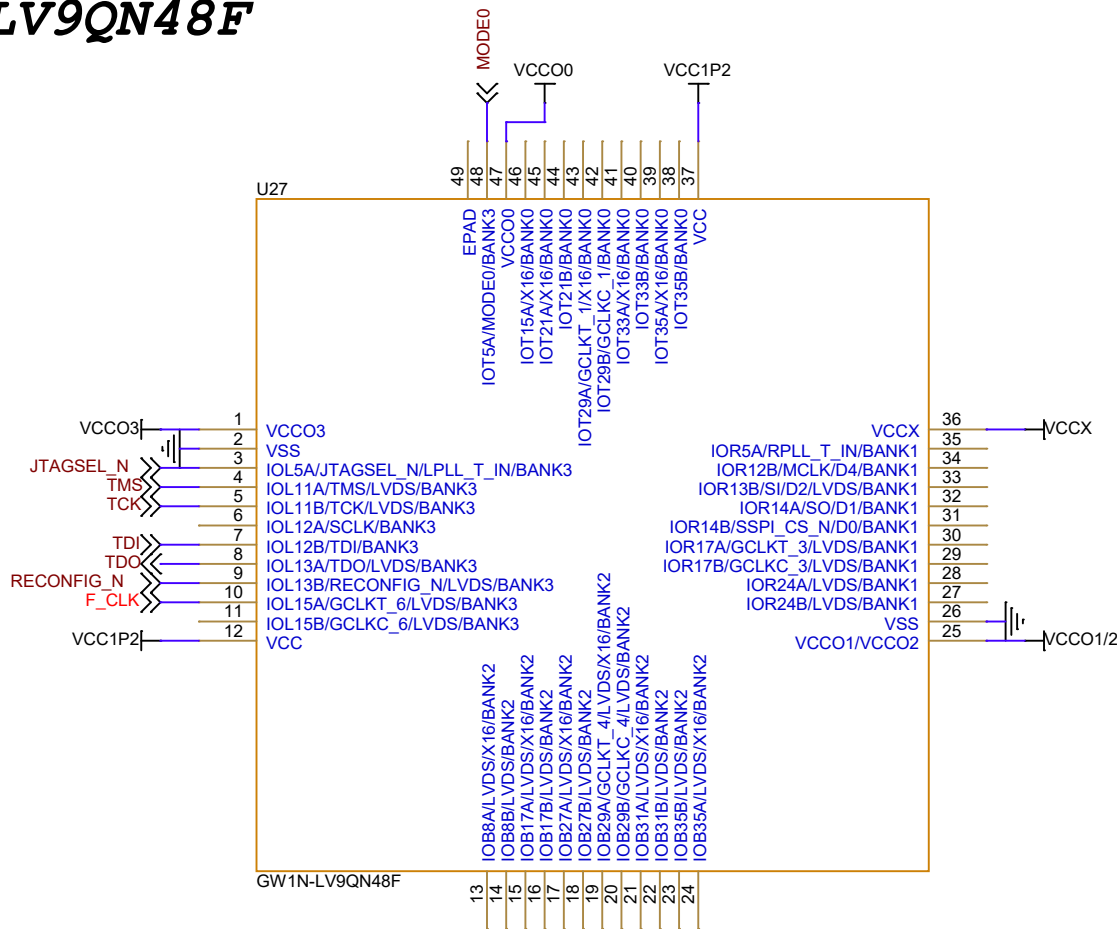
Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-LV9QN48F



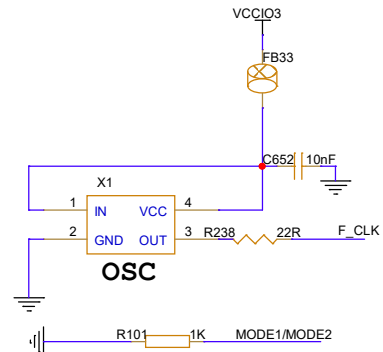
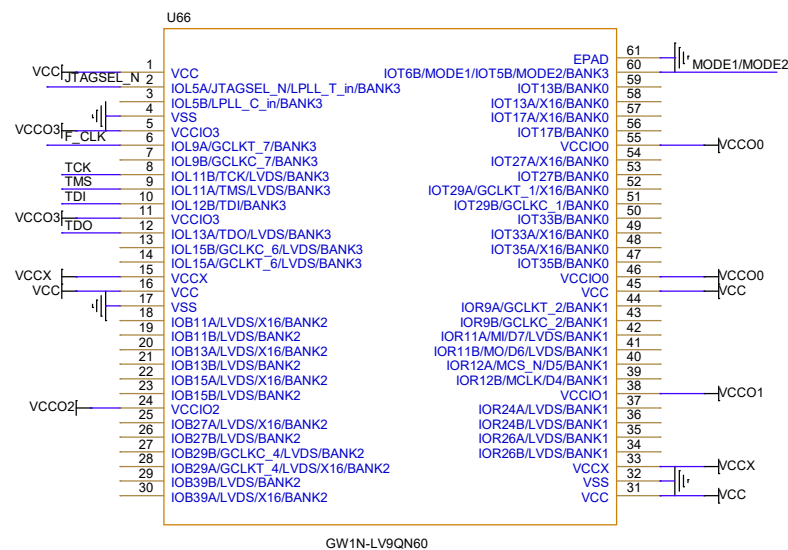
Notes:

1.F CLK signal is an external input clock signal.

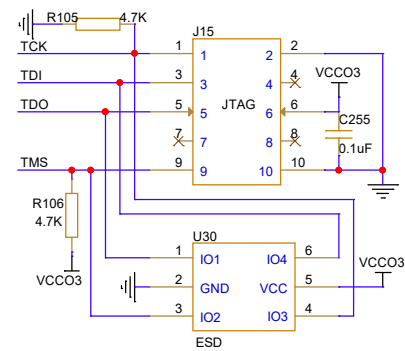
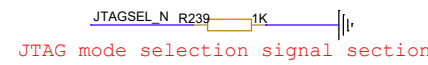
It is recommended that F CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

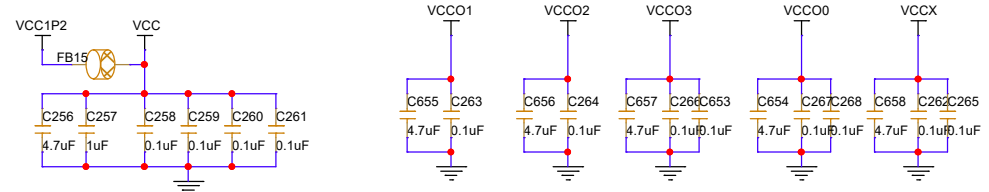
Title		
GOWIN Minimum System Diagram		
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A4	GW1N-LV9QN48F	2.3
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*Configuration mode signal selection section
MODE0 has already been grounded within the chip.

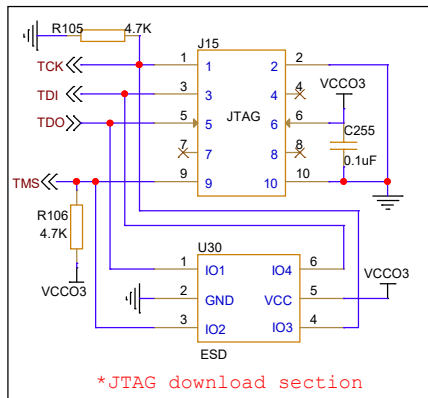
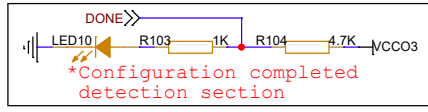
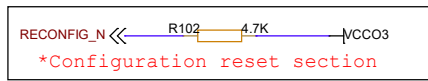
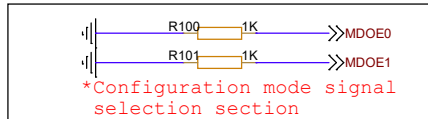
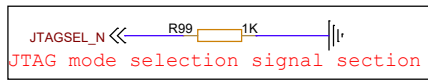
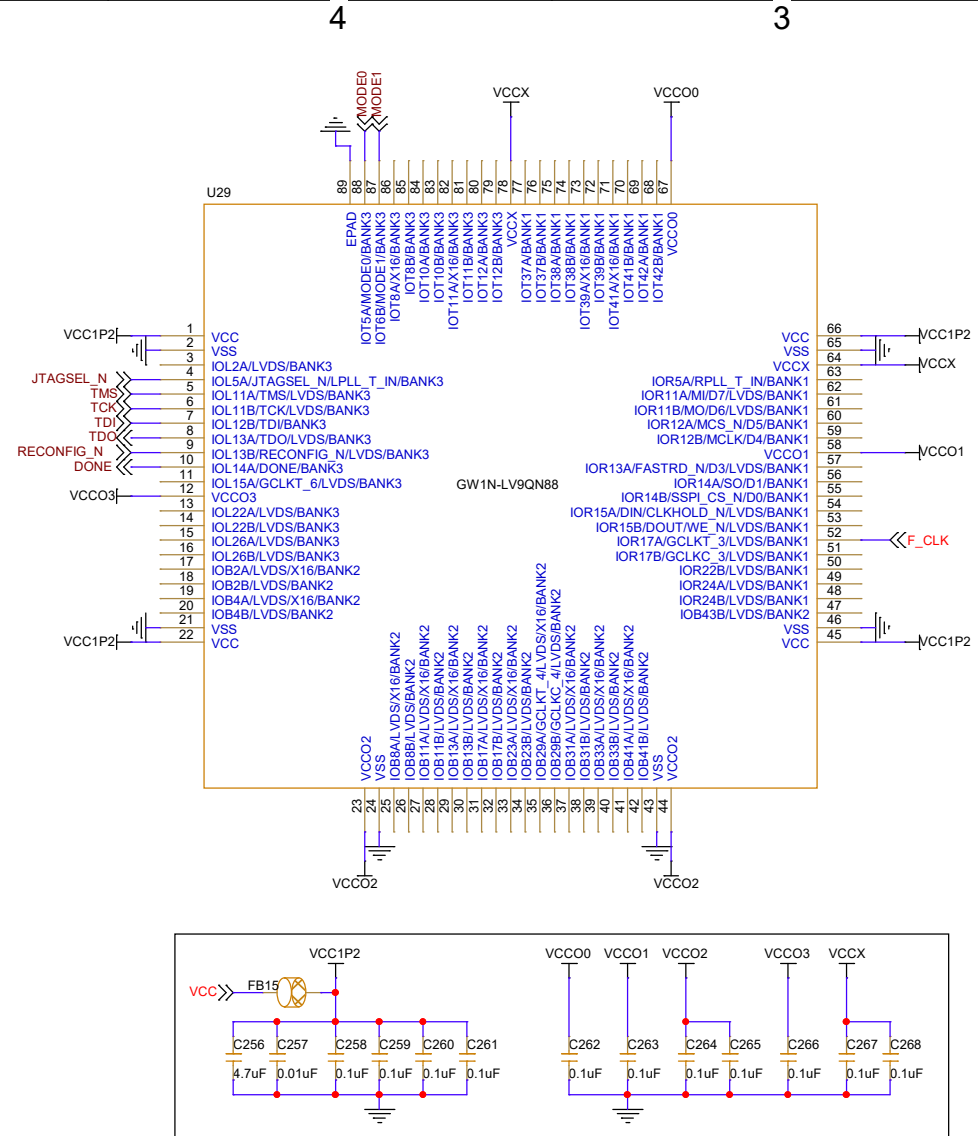


*JTAG download section



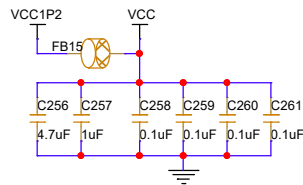
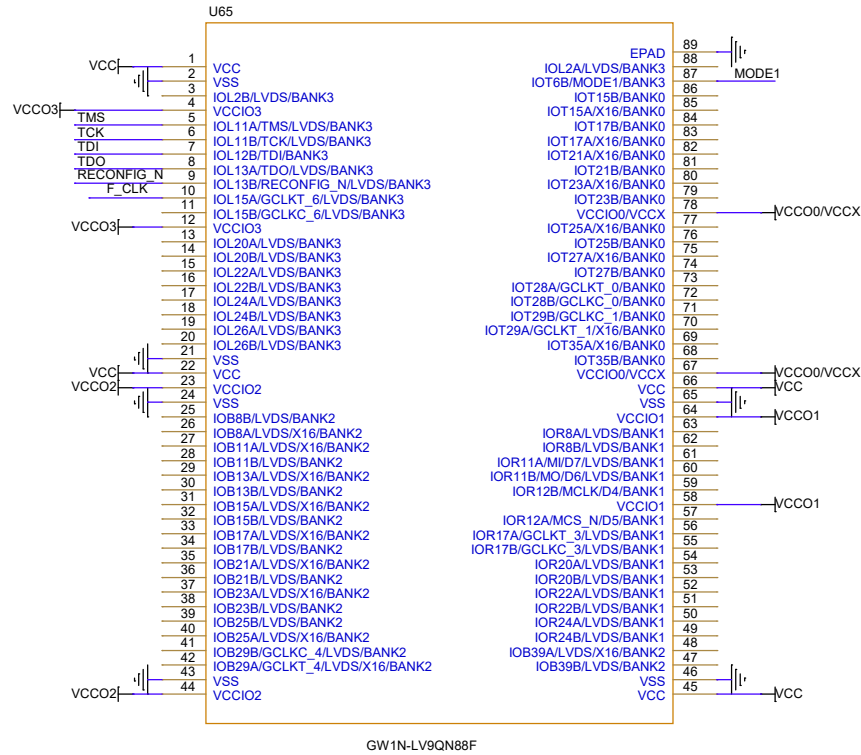
- Notes:
- 1.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 2.VCCX must not be less than the maximum VCCIO.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN60	1.0
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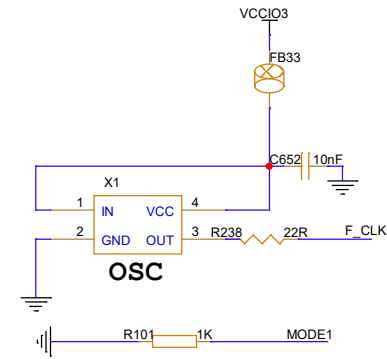
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
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B	GW1N-LV9QN88	2.3
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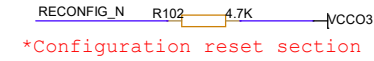


Notes:

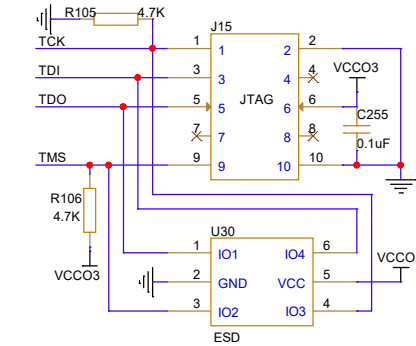
1. It is recommended that add an ESD protection chip to the JTAG download circuit.
2. VCCX must not be less than the maximum VCCIO.



*Configuration mode signal selection section
MODE0 and MODE2 have already been grounded within the chip.

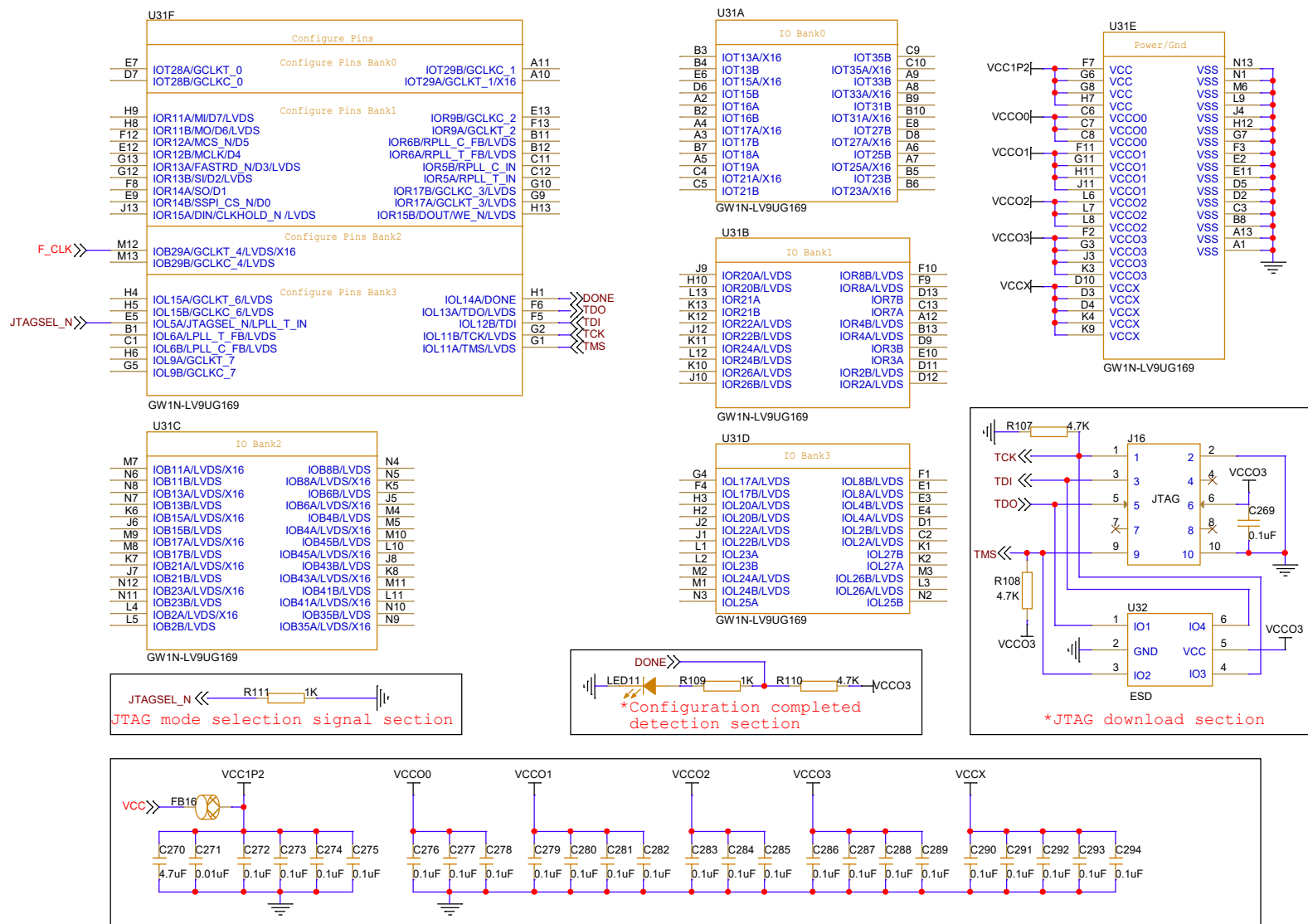


*Configuration reset section



*JTAG download section

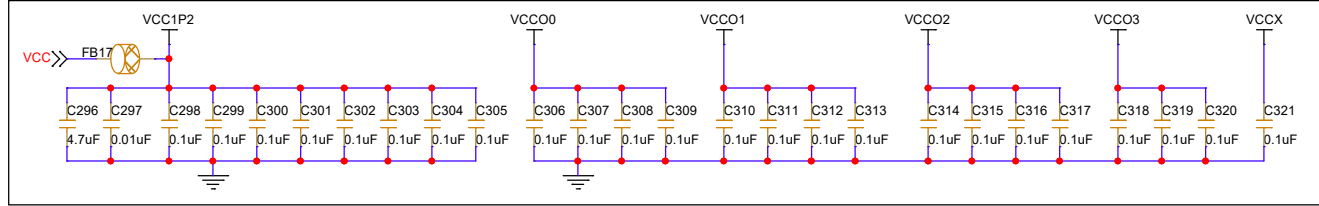
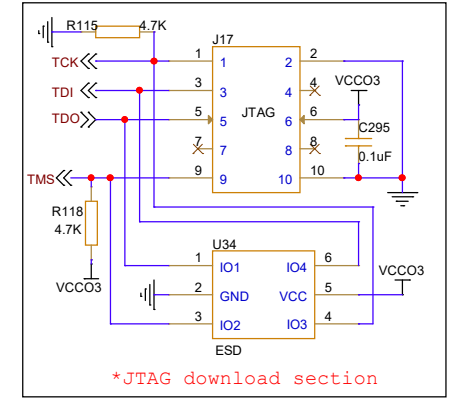
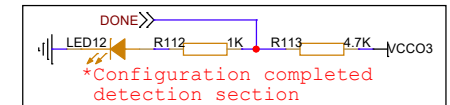
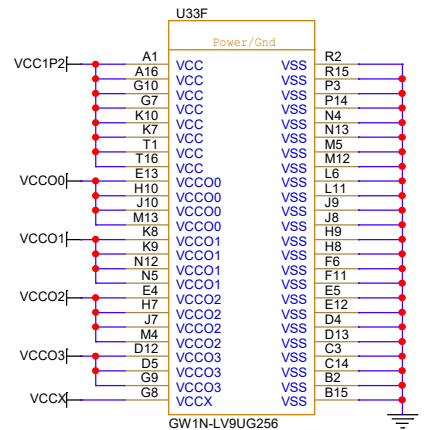
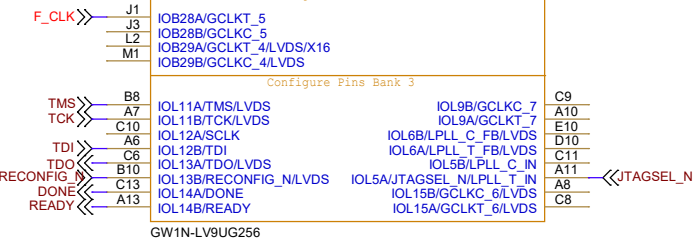
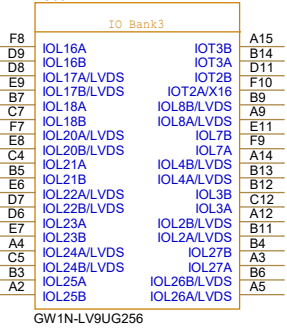
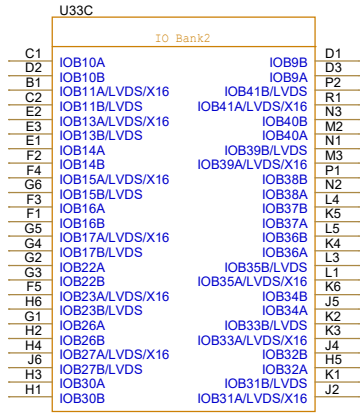
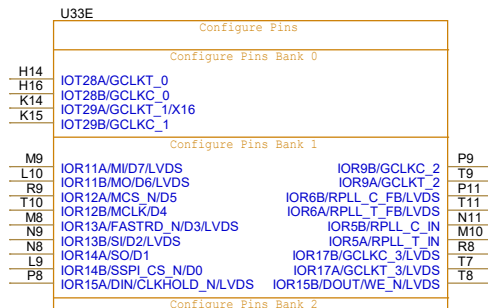
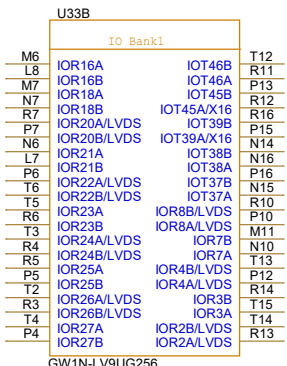
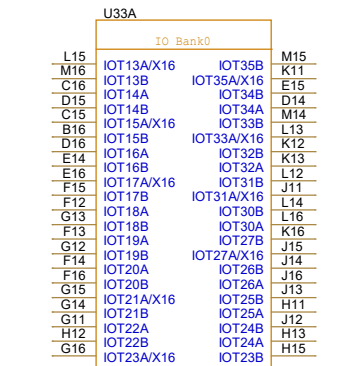
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9QN88F	1.0
Date:	Thursday, February 26, 2026	Sheet 15 of 32



Notes:

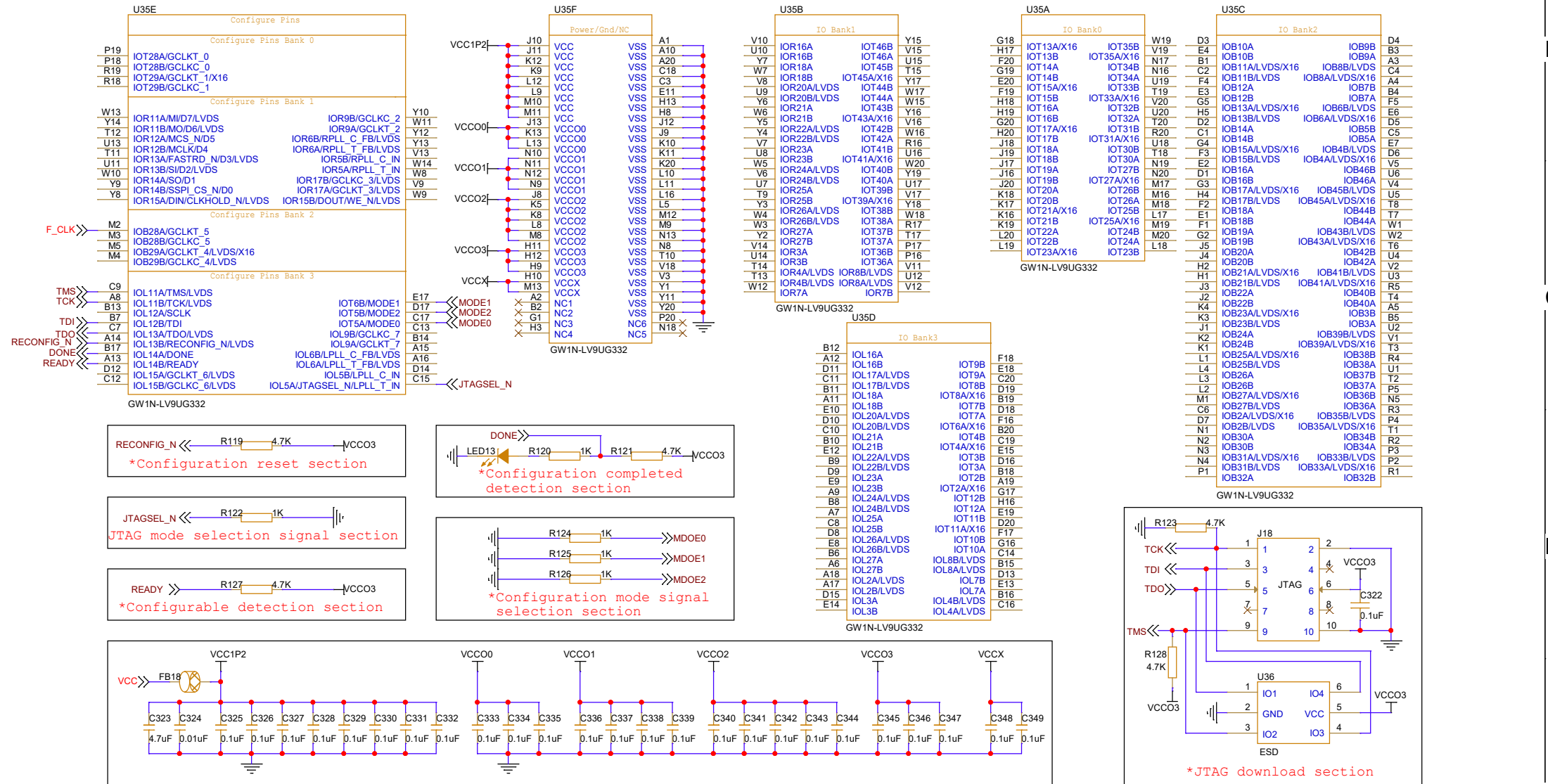
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title				
GOWIN Minimum System Diagram				
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Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9UG256	2.3
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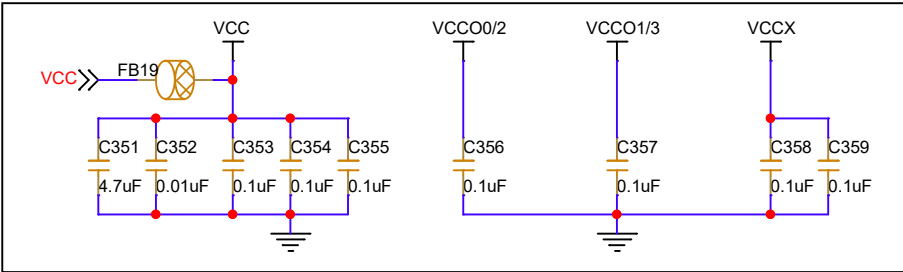
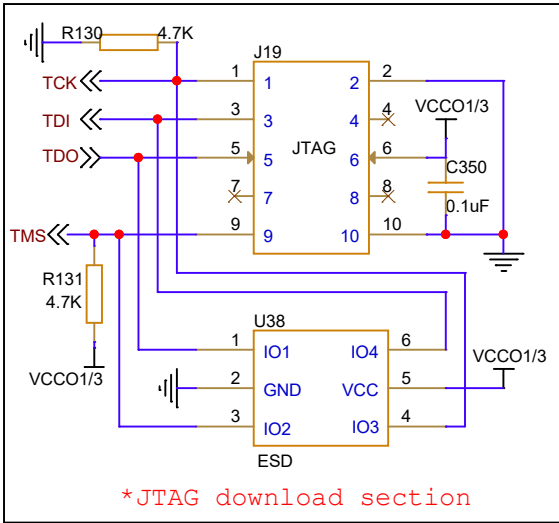
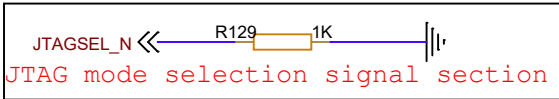
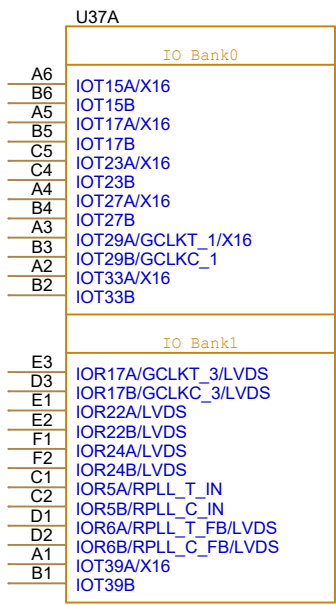
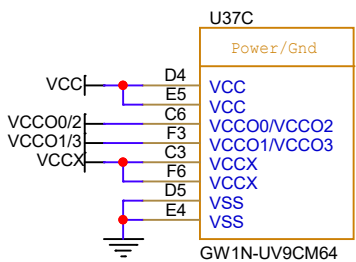
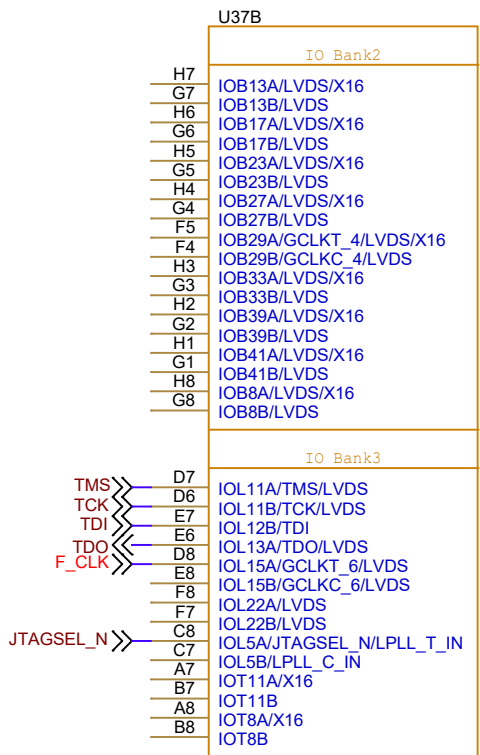


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV9UG332	2.3
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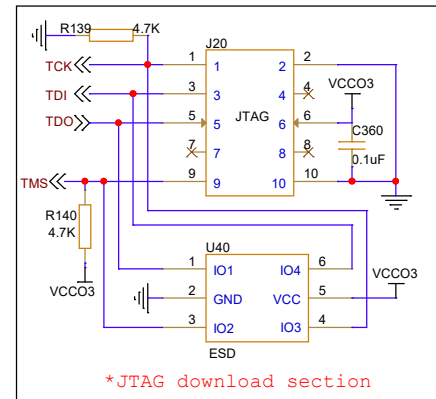
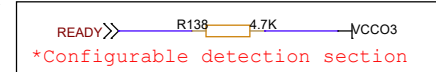
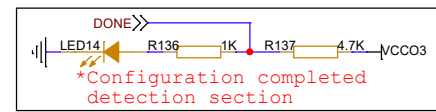
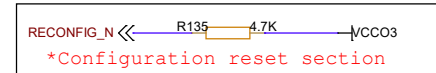
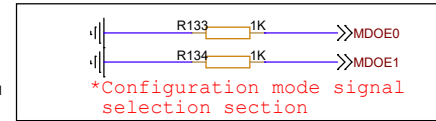
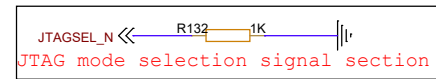
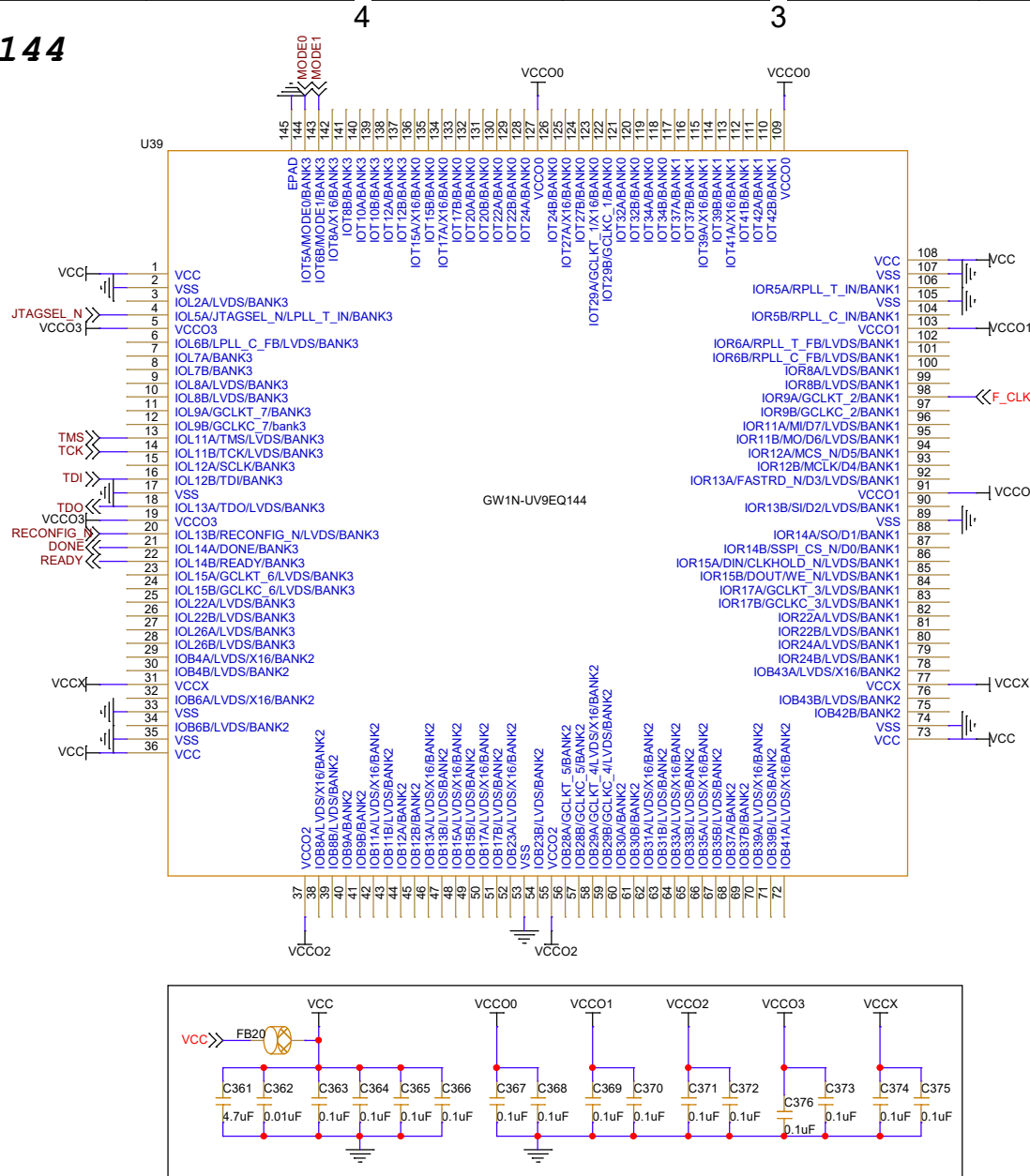
GW1N-UV9CM64



Notes:

1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.

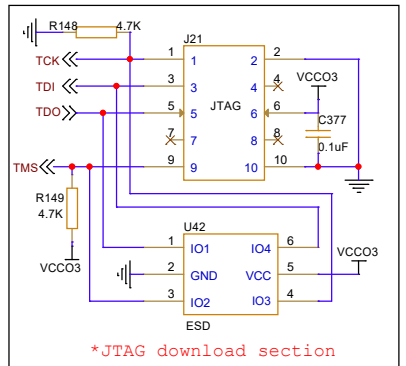
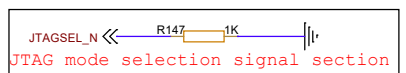
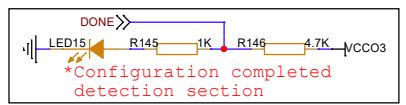
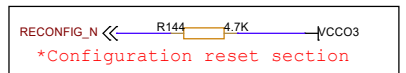
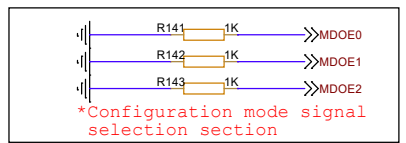
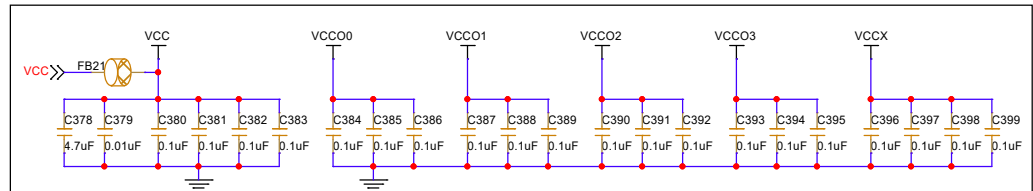
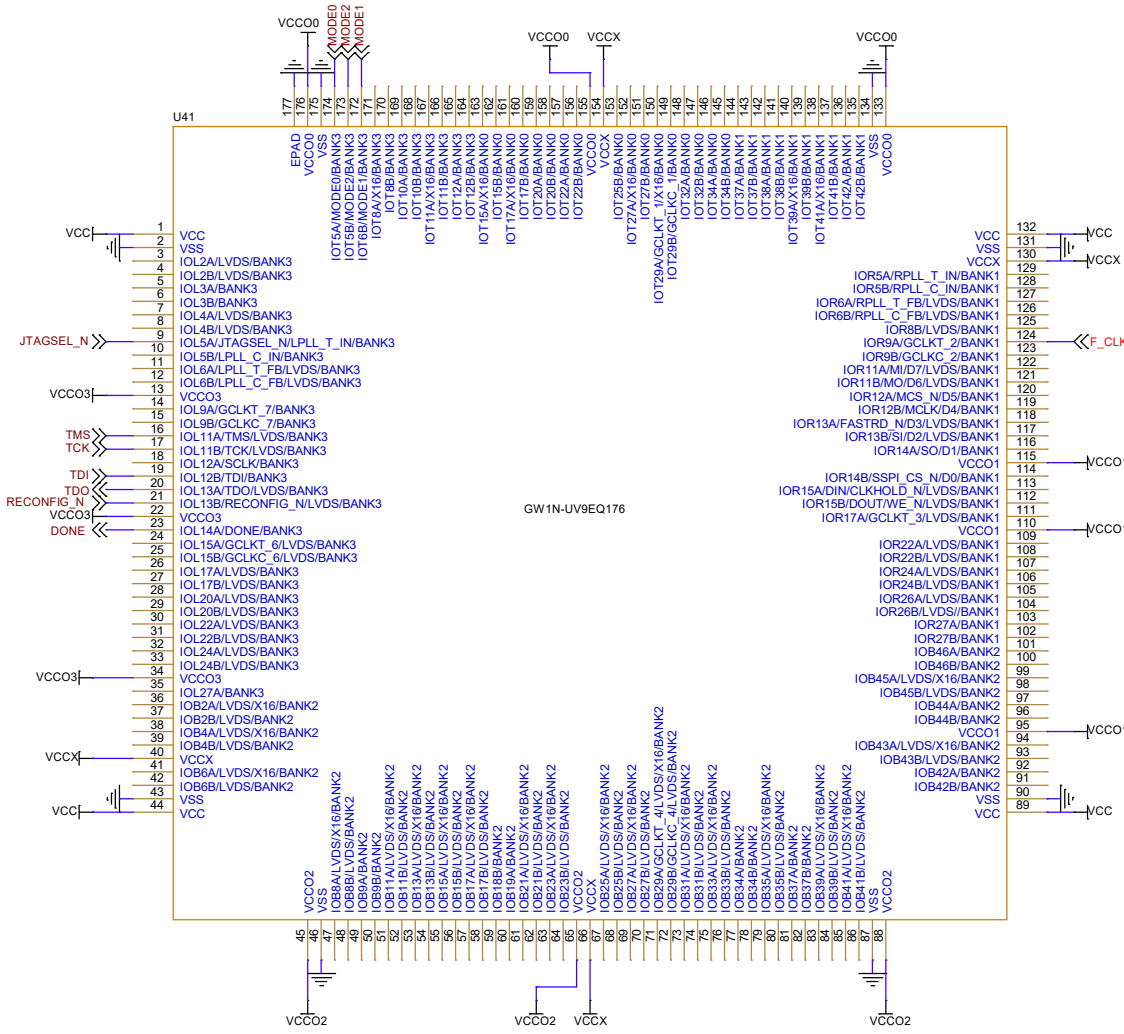
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



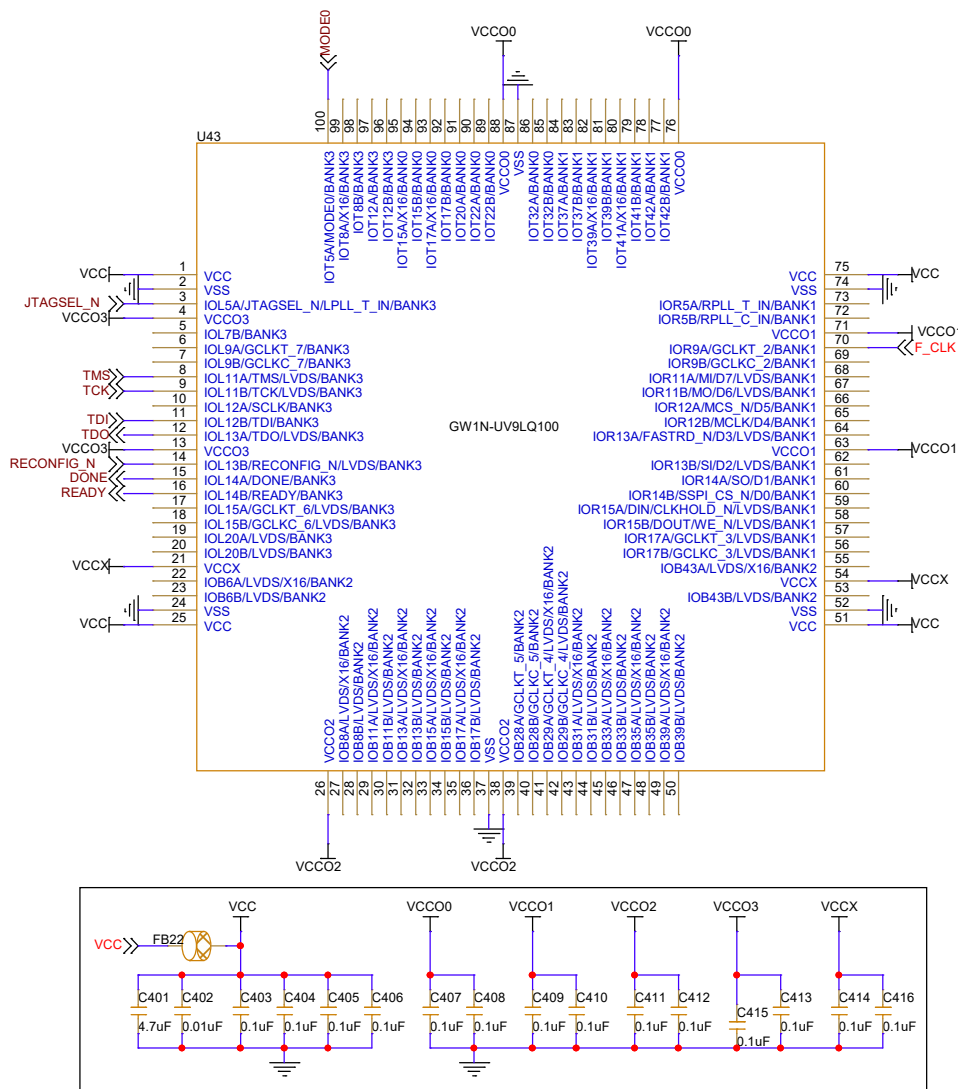
Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV9EQ144	Rev 2.3
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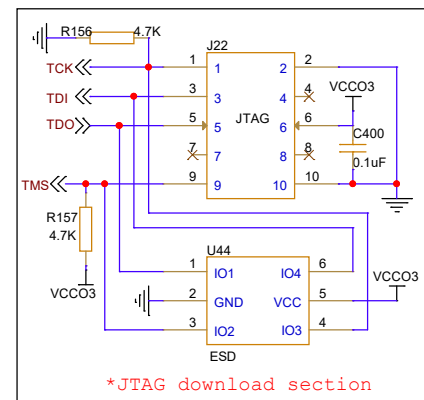
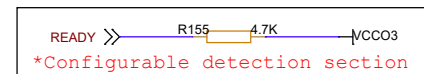
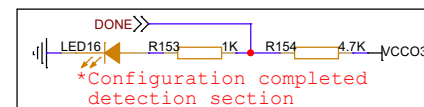
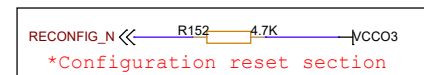
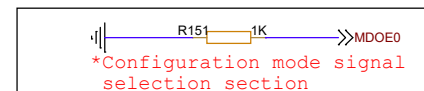
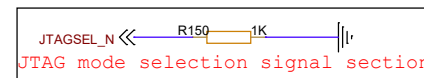


Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection to the JTAG download circuit.

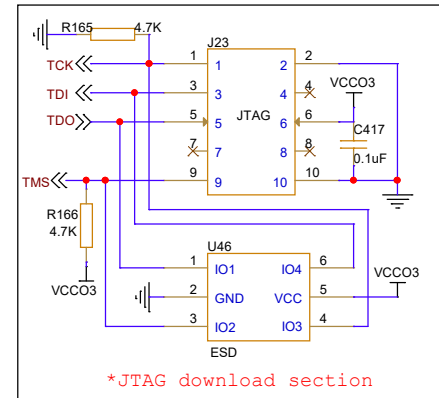
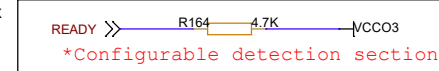
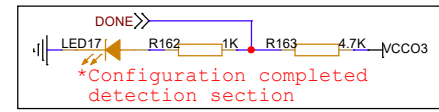
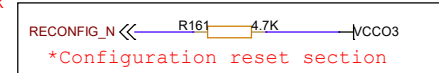
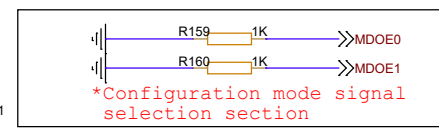
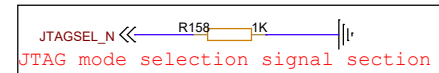
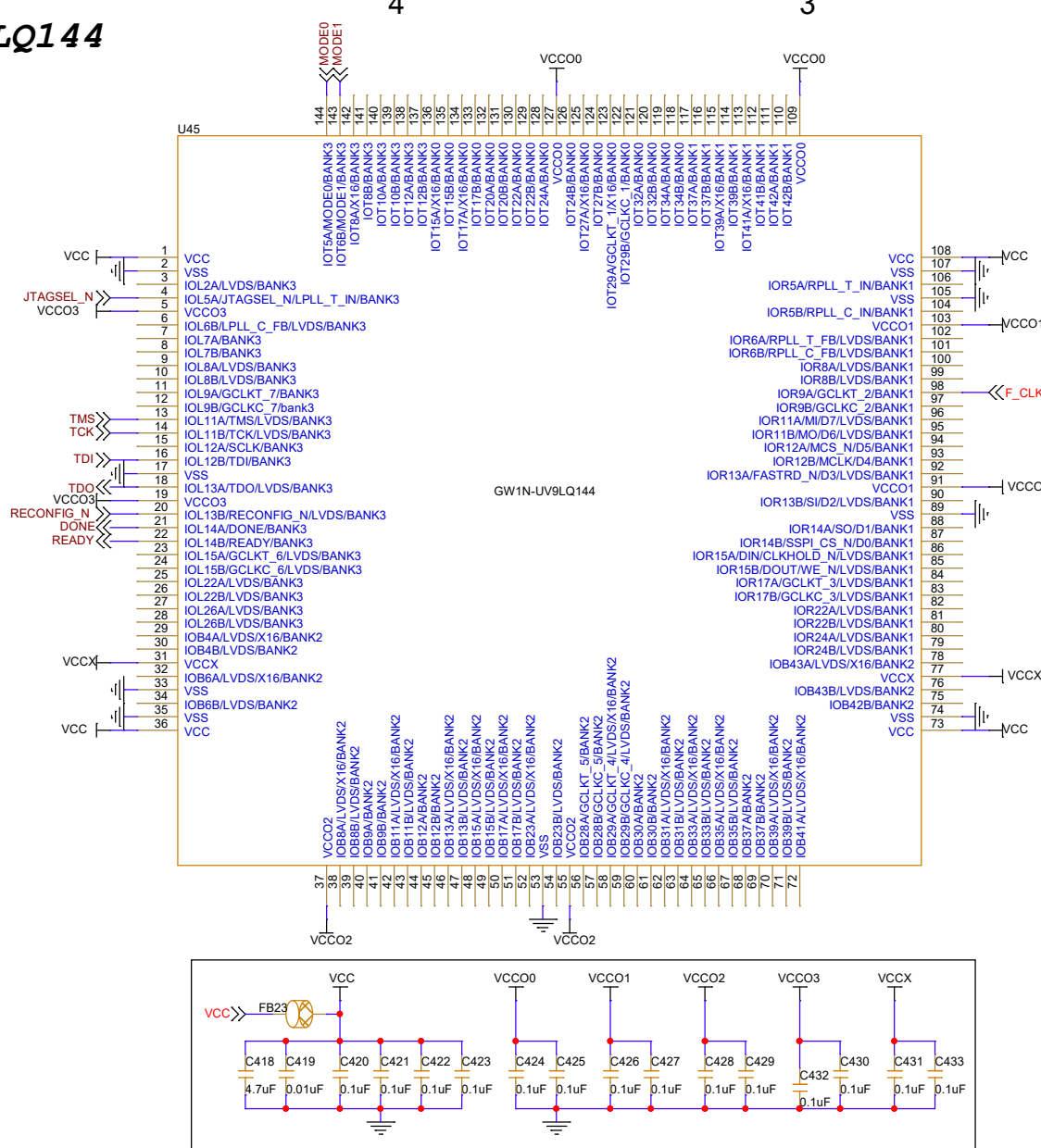


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



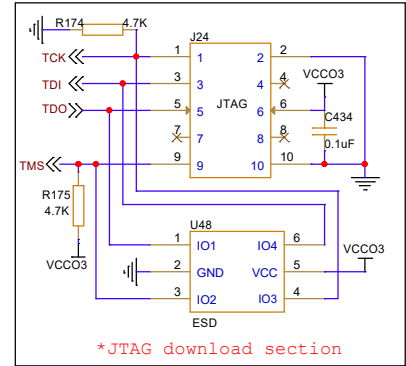
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Size	Document Number	Rev
B	GW1N-UV9LQ100	2.3
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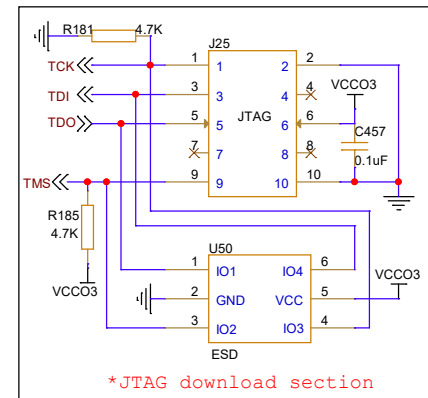
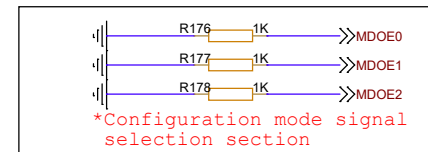
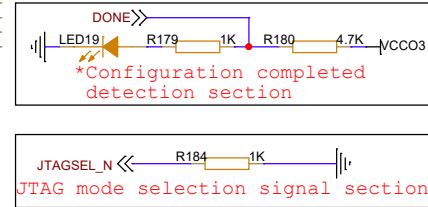
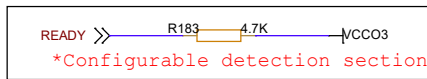
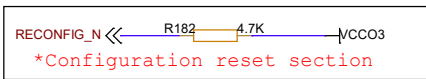
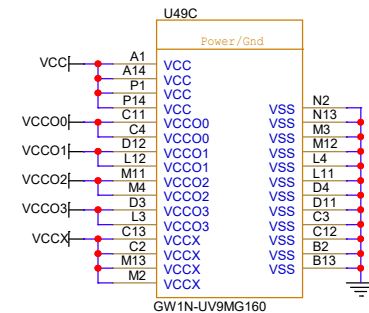
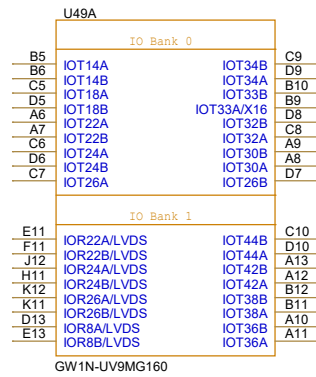
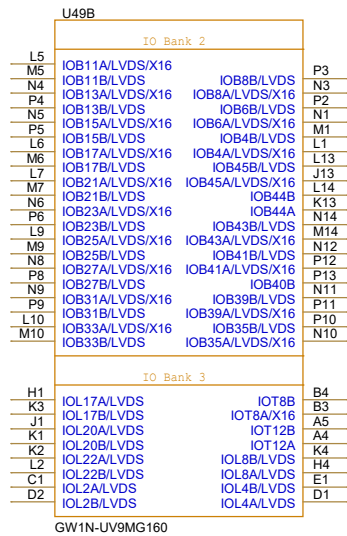
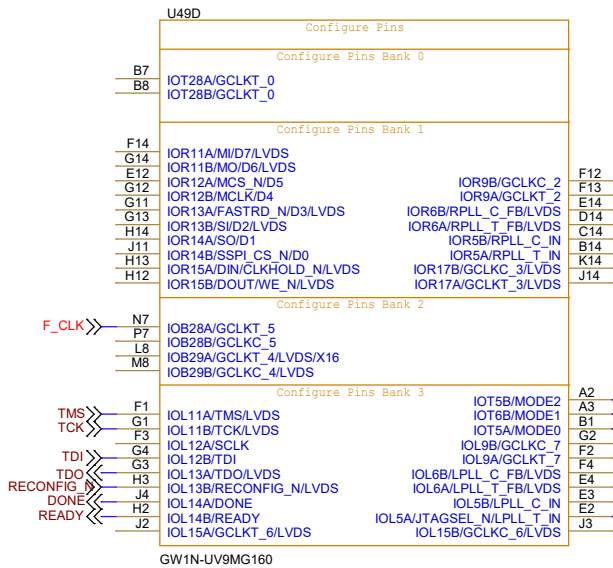
Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
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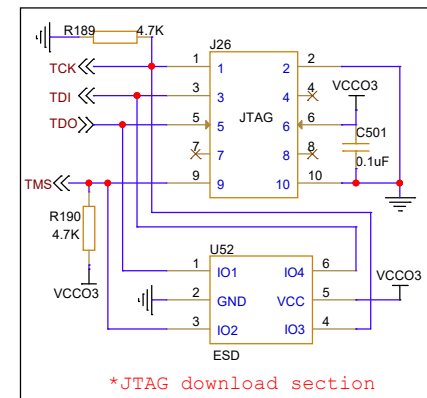
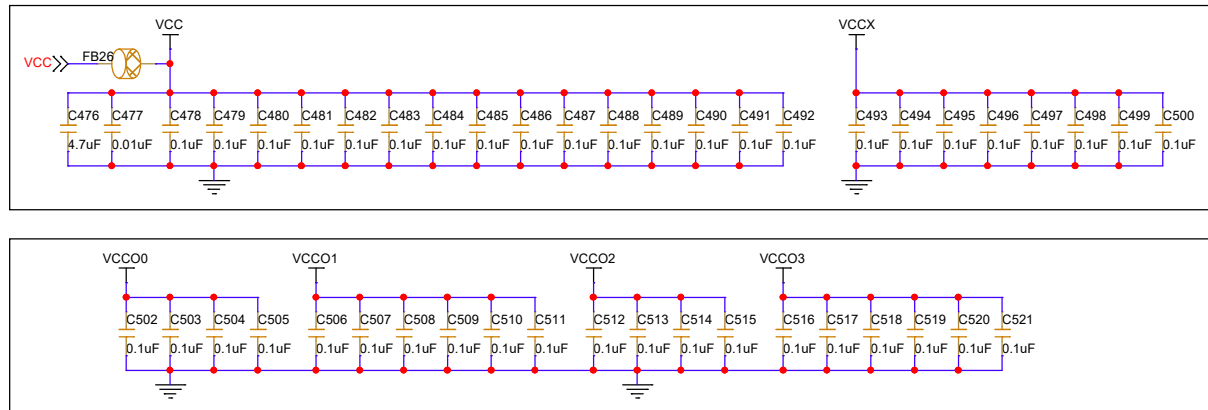
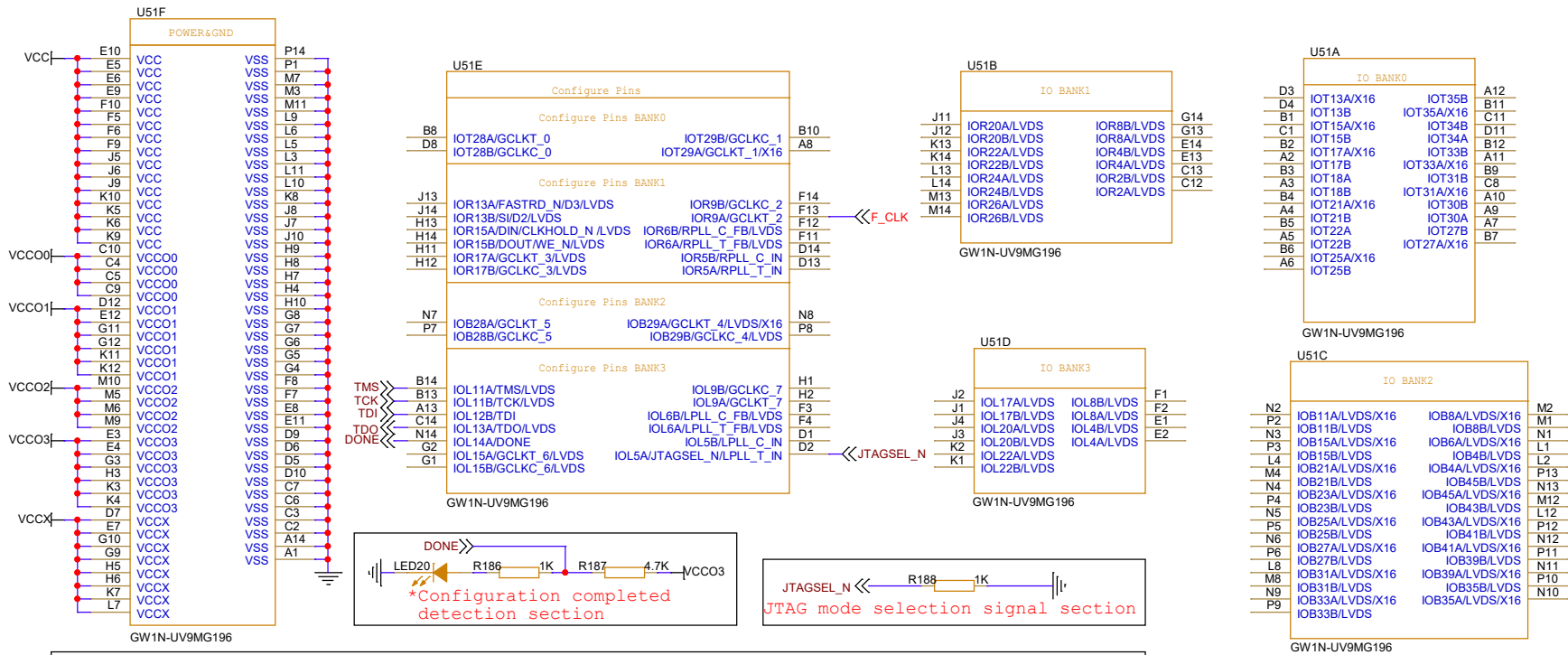


Title				
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Size	Document Number			Rev
A3	GW 1N-UV9LQ176			2.3
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Notes:

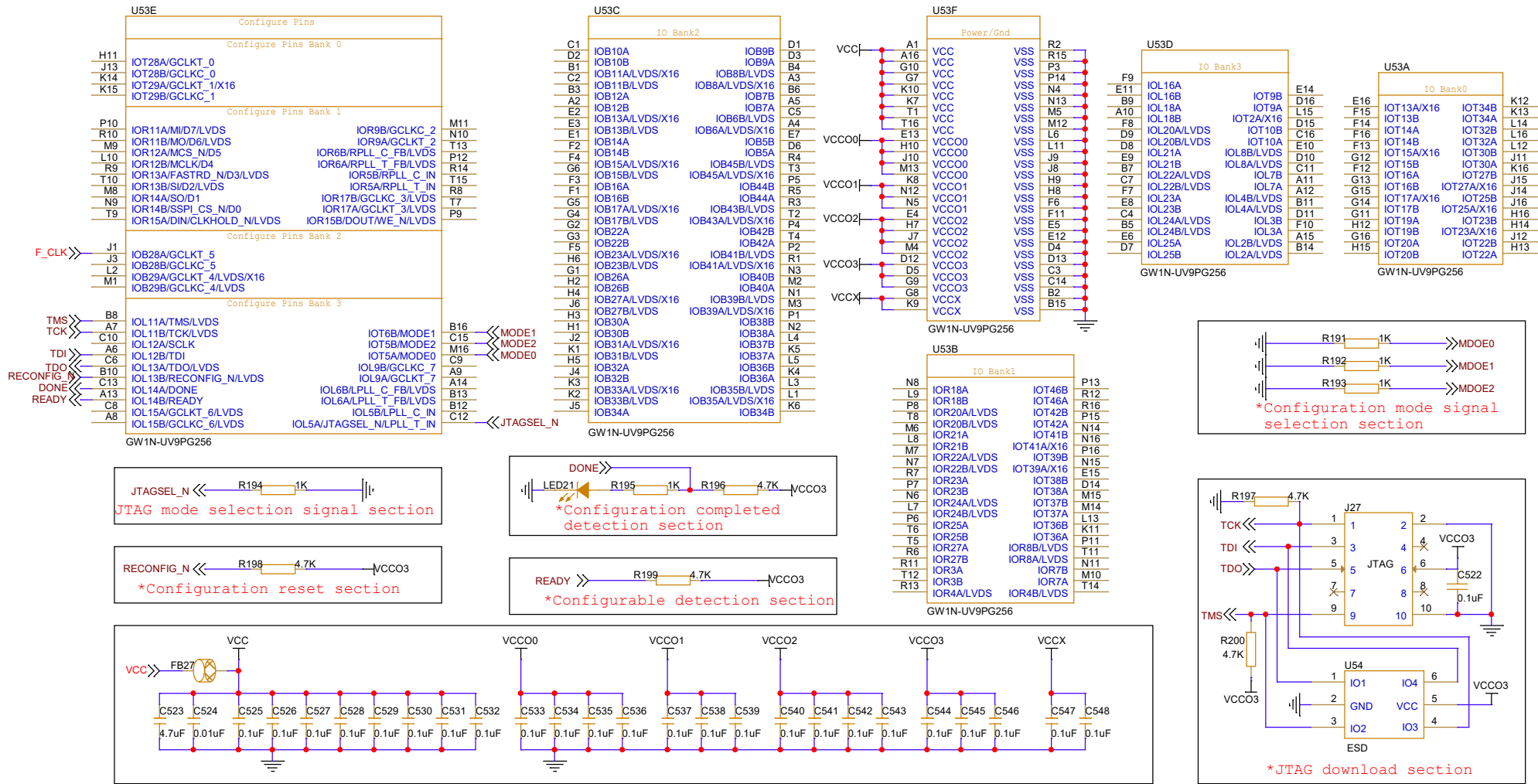
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV9MG196	Rev 2.3
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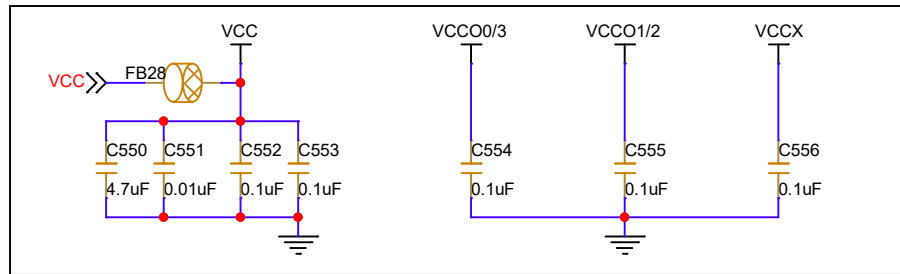
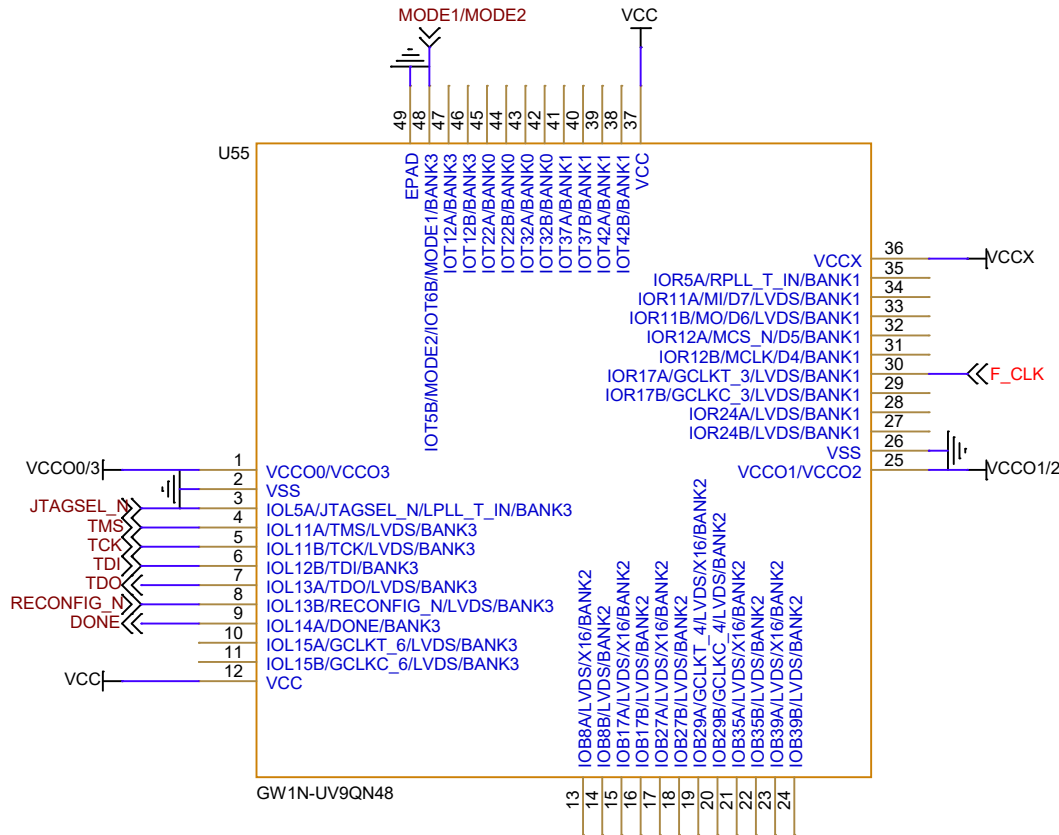


Notes:

1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV9PG256	2.3
Date:	Tuesday, April 22, 2025	Sheet 27 of 32

GW1N-UV9QN48

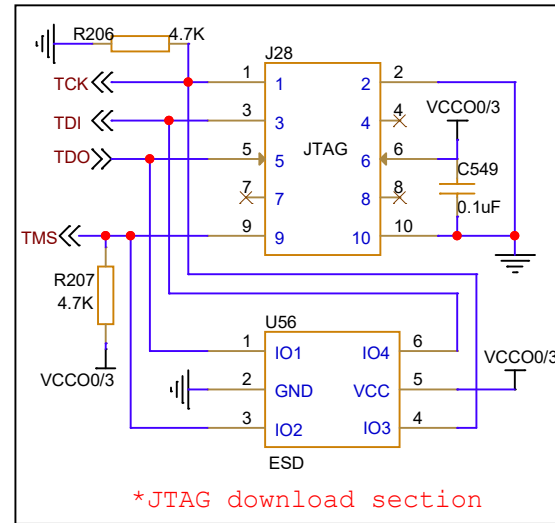
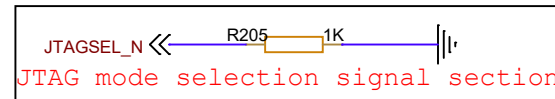
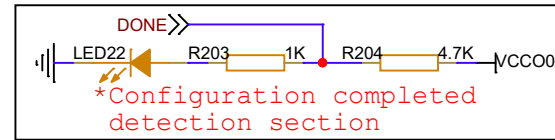
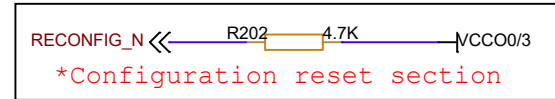
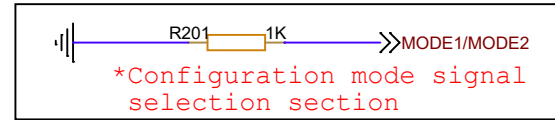


Notes:

1.F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Title
GOWIN Minimum System Diagram

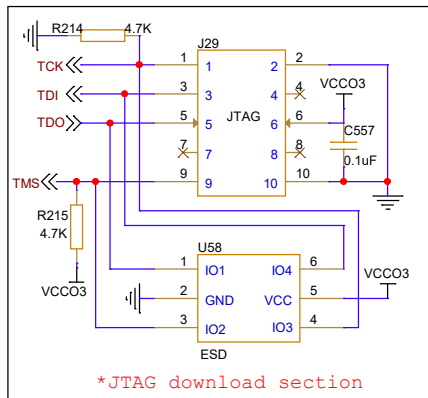
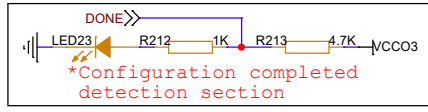
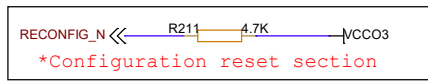
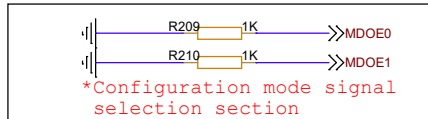
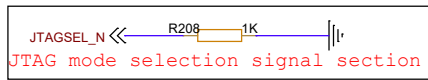
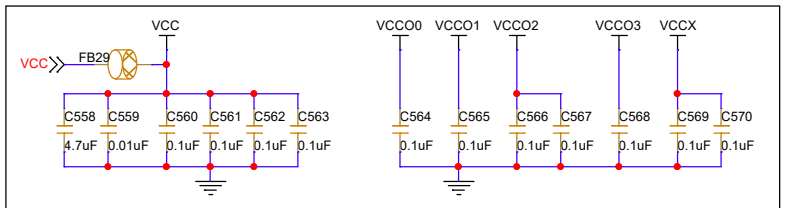
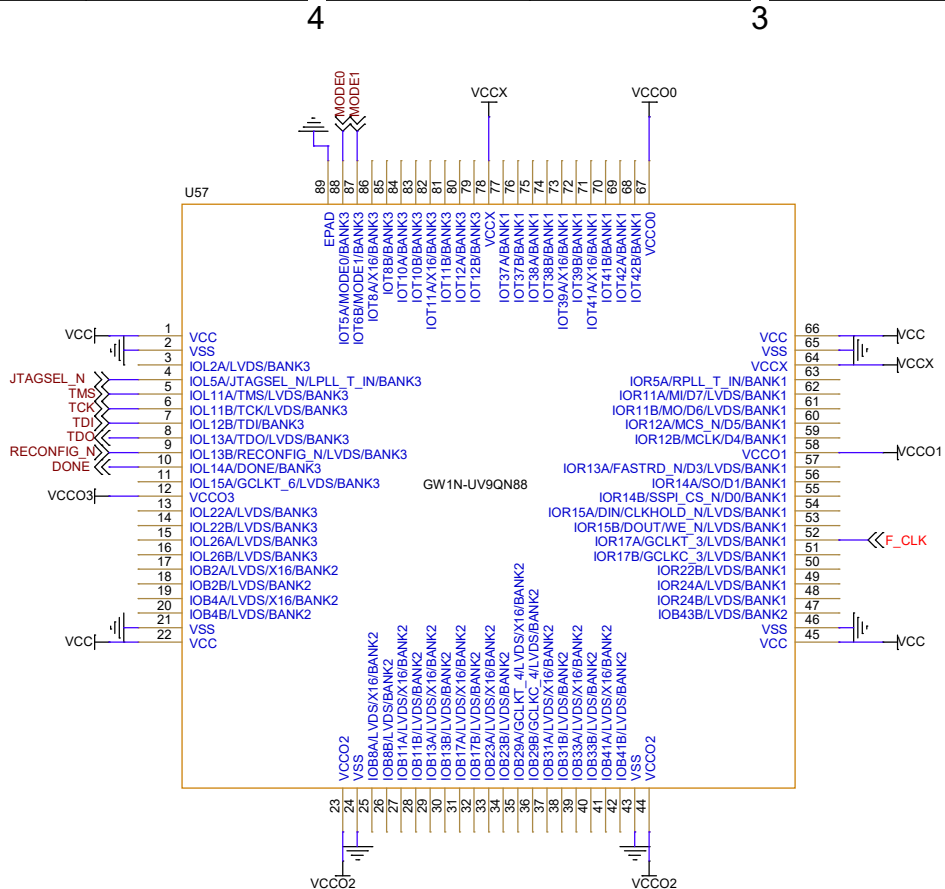
Size
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Document Number
GW1N-UV9QN48

Rev
2.3

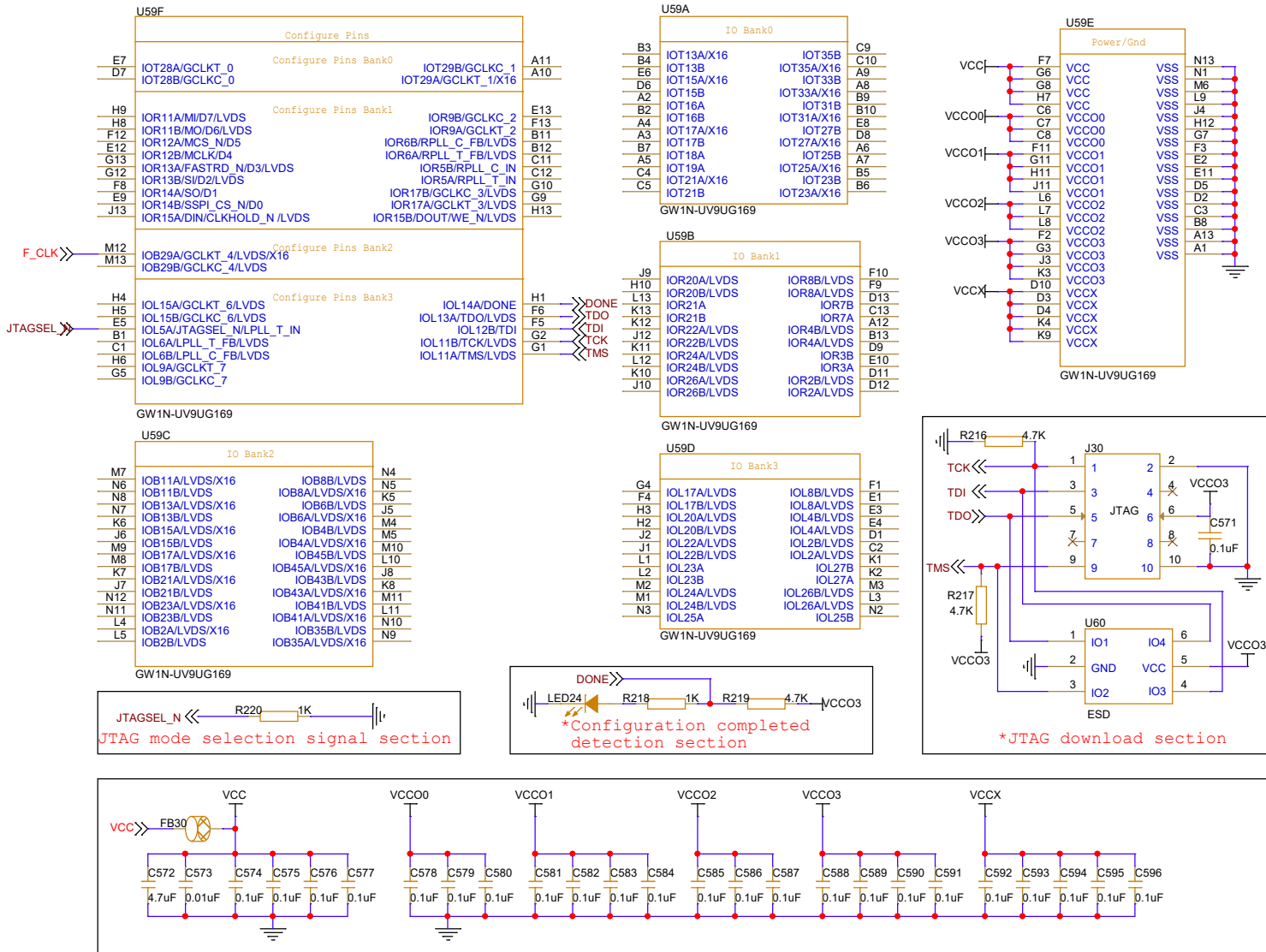
Date: Tuesday, April 22, 2025

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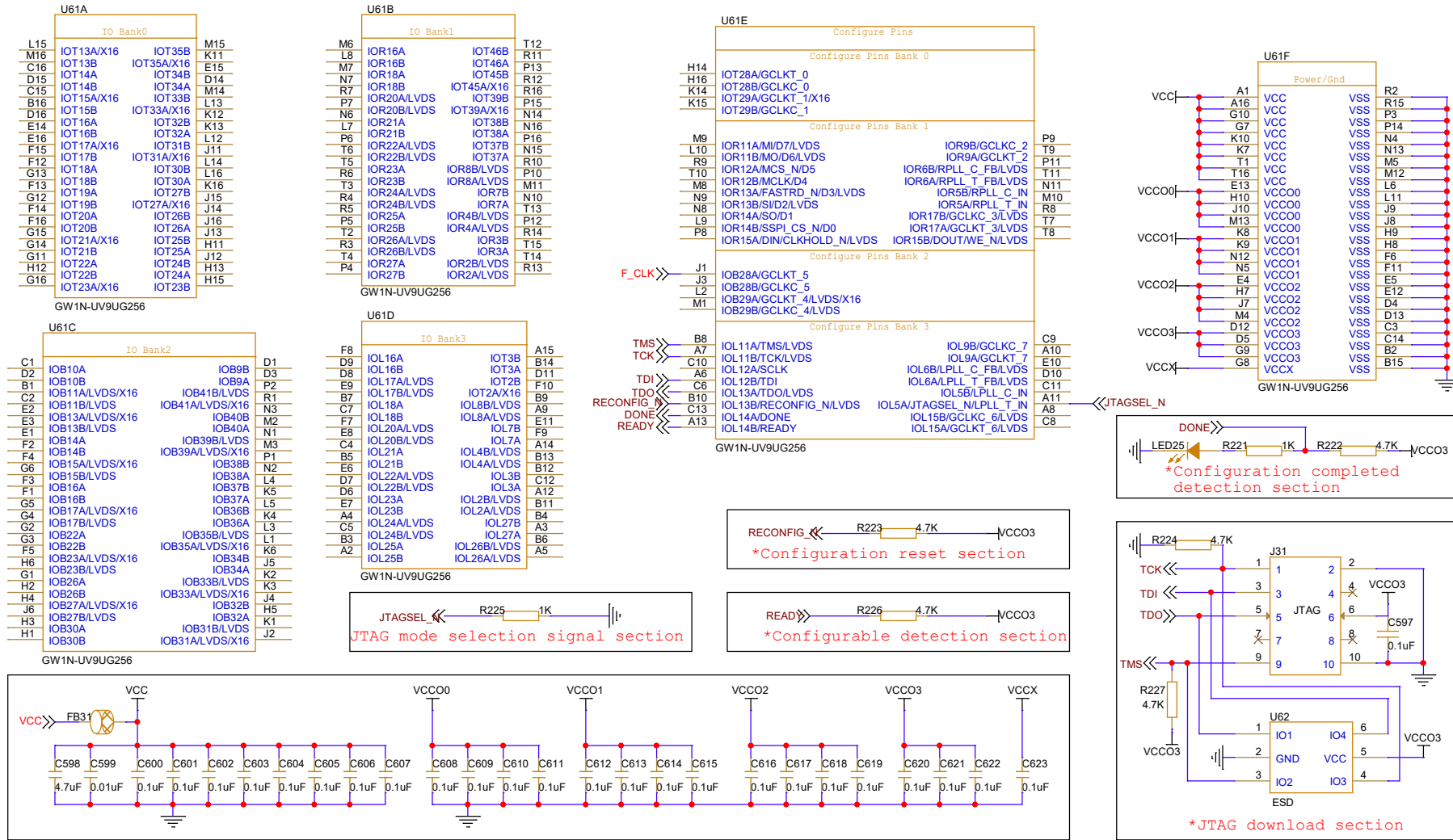
Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV9QN88	Rev 2.3
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Notes:
1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

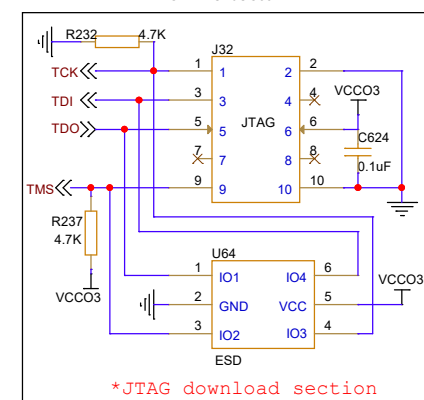
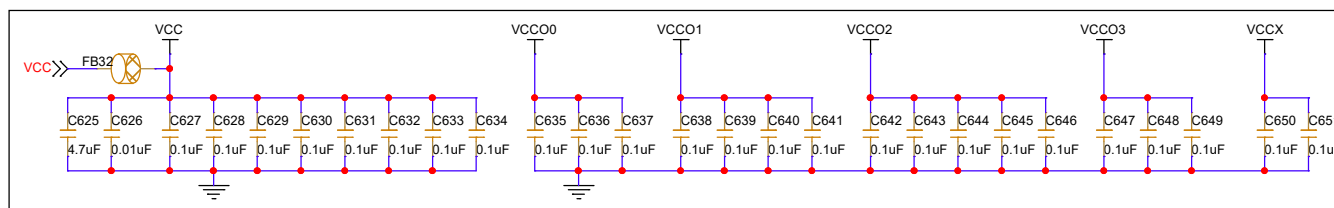
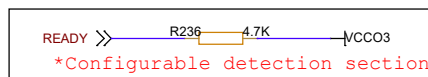
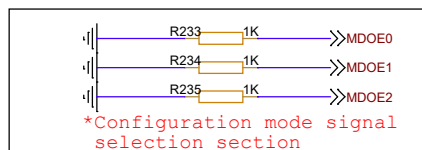
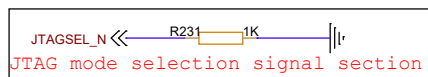
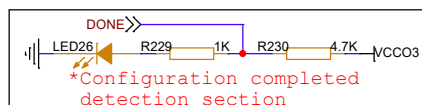
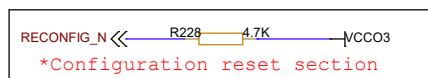
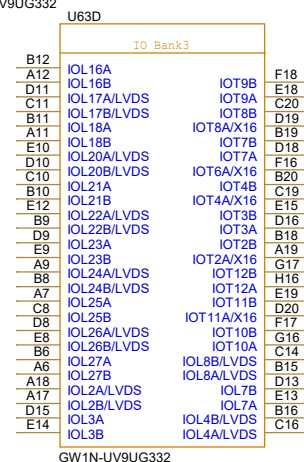
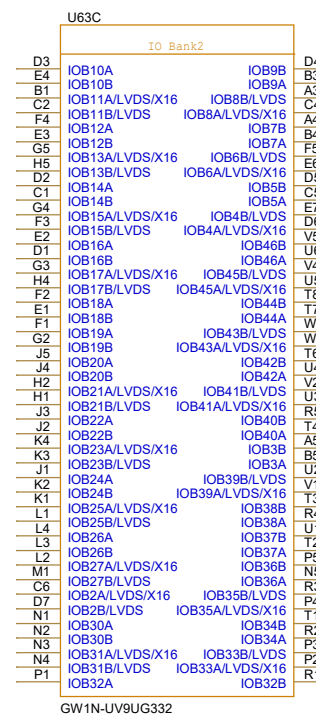
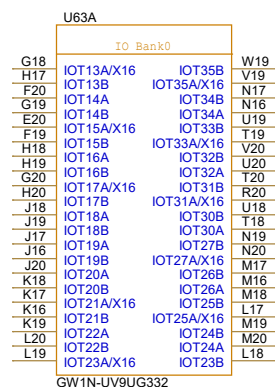
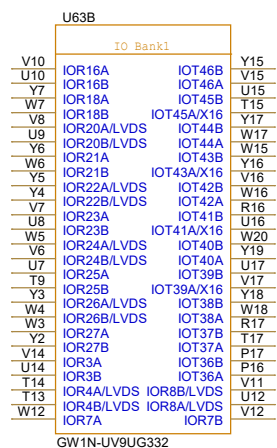
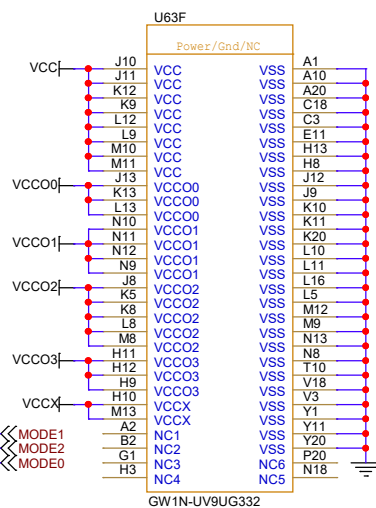
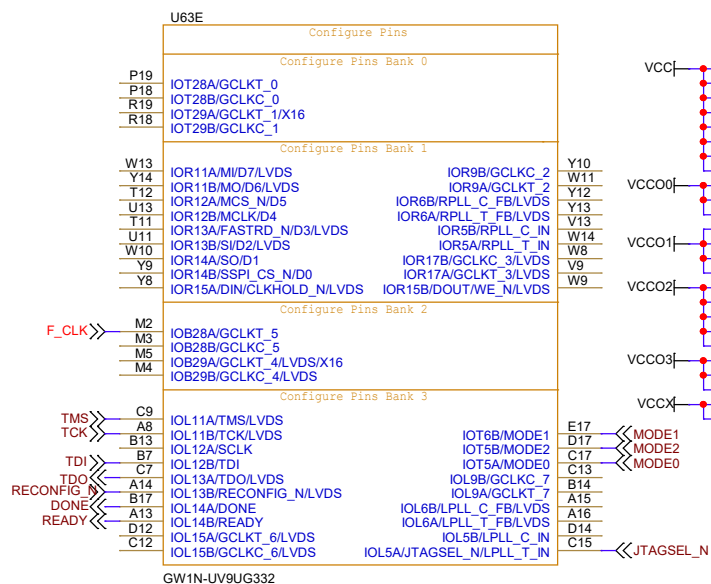
Title		
GOWIN Minimum System Diagram		
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Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

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GOWIN Minimum System Diagram		
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Notes:

- NOTES:
- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title				
GOWIN Minimum System Diagram				
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